Release Note

SSP v1.7.0

Release Note

Renesas Synergy™ Platform
Synergy Software
Synergy Software Package

Renesas Electronics
www.renesas.com

Rev.1.01 Sep 2019

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Renesas Synergy™ Platform

SSP v1.7.0 Release Note

Contents

1. Introduction

This document describes the release notes for **Synergy Software Package (SSP) version 1.7.0**.

2. Release Information

SSP Release Version	v1.7.0
Release Date	September 10, 2019

The intended audience for this release note is Renesas Synergy™ customers, prospective customers, partners, and support staff. This release note describes the fixed issues and known issues in SSP v1.7.0.

3. Synergy MCU Groups Supported

MCU Groups: S7G2, S5D9, S5D5, S5D3, S3A7, S3A6, S3A3, S3A1, S128, S124, and S1JA.

4. Software Tools and Hardware Kits Supported with this SSP Release

Tool	Version	Description
e^2 studio	7.5.1	Software development and debugging tool. Link: www.renesas.com/synergy/tools
IAR Embedded Workbench® for Renesas Synergy™	8.23.3.18530	Software development environment and debugging tool. Link: www.renesas.com/synergy/tools
SSC	7.5.1	Synergy Standalone Configurator. Used in combination with IAR EW for Synergy. Link: www.renesas.com/synergy/tools
GNU Arm Compiler	7.2.1 and 4.9.3	Both versions of GNU Arm® compilers are supported with SSP v1.7.0 Note 1: GCC 4.9.3 does not support S1JA MCU Group. Note 2: GCC 4.9 does not support S1JA MCU Group (Arm® Cortex®-M23 core)
IAR Compiler	8.23.3.18530	IAR Arm® compiler toolchain
PE-HMI1	2.0	Product Example (PE) for Human Machine Interface to evaluate Renesas Synergy™ S7G2 MCU Group
DK-S7G2	4.1	Development Kit for Renesas Synergy™ S7G2 MCU Group
SK-S7G2	3.3	Starter Kit for Renesas Synergy™ S7G2 MCU Group
PK-S5D9	1.0	Promotion Kit for Renesas Synergy™ S5D9 MCU Group
TB-S5D5	1.1	Target Board Kit for Renesas Synergy™ S5D5 MCU Group
TB-S5D3	1.0	Target Board Kit for Renesas Synergy™ S5D3 MCU Group
DK-S3A7	2.0	Development Kit for Renesas Synergy™ S3A7 MCU Group
TB-S3A6	1.0	Target Board Kit for Renesas Synergy™ S3A6 MCU Group
TB-S3A3	1.0	Target Board Kit for Renesas Synergy™ S3A3 MCU Group
TB-S3A1	1.0	Target Board Kit for Renesas Synergy™ S3A1 MCU Group
DK-S128	1.1	Development Kit for Renesas Synergy™ S128 MCU Group
DK-S124	3.1	Development Kit for Renesas Synergy™ S124 MCU Group
TB-S1JA	1.2	Target Board Kit for Renesas Synergy™ S1JA MCU Group

Tool	Version	Description
J-Link Software	6.34e	SEGGER J-Link® debug probe is the quasi standard for Arm® Cortex®-M based MCUs

4.1 Version Information for Third-Party Products

Component	Version in SSP v1.7.0
ThreadX®	5.8 SP4
NetX™	5.11 SP1
NetX Duo™	5.11 SP1
NetX Application bundle	5.11 SP1
NetX Duo Application bundle	5.11 SP1
NetX Web HTTP/HTTPS	5.11 SP1
USBX™ Host	5.8 SP6
USBX™ Device	5.8 SP6
FileX®	5.5 SP1
GUIX™	5.4.1
LevelX	5.4
TraceX®	5.2.0
GUIX Studio™	5.4.2.9
NetX Secure	5.11 SP2
MQTT for NetX Duo	5.11 SP1
SNMP for NetX	5.11 SP1
SNMP for NetX Duo	5.11 SP1
TES D/AVE 2D	3.17

5. SSP Release Package and Installation Information

Before installing SSP standalone installer, ensure that the following items are installed on your PC:

- **Renesas e² studio ISDE v7.5.1** (download and install the e² studio Installer from the Renesas website at www.renesas.com/synergy/software)
- **GNU Arm® Compiler** (included with Renesas e² studio ISDE v7.5.1)

To install the SSP, follow these steps:

1. Download the following items for the SSP Release from www.renesas.com/synergy/software:
   - **SSP_Distribution_1.7.0.zip** (SSP Package Installer, including SSP Package)
   - **Renesas Synergy Software Package (SSP) v1.7.0 Release Note**.
2. Unzip the package and run the **SSP_Distribution_1.7.0.exe** installer.
3. Install the SSP in the root folder of a compatible e² studio installation.

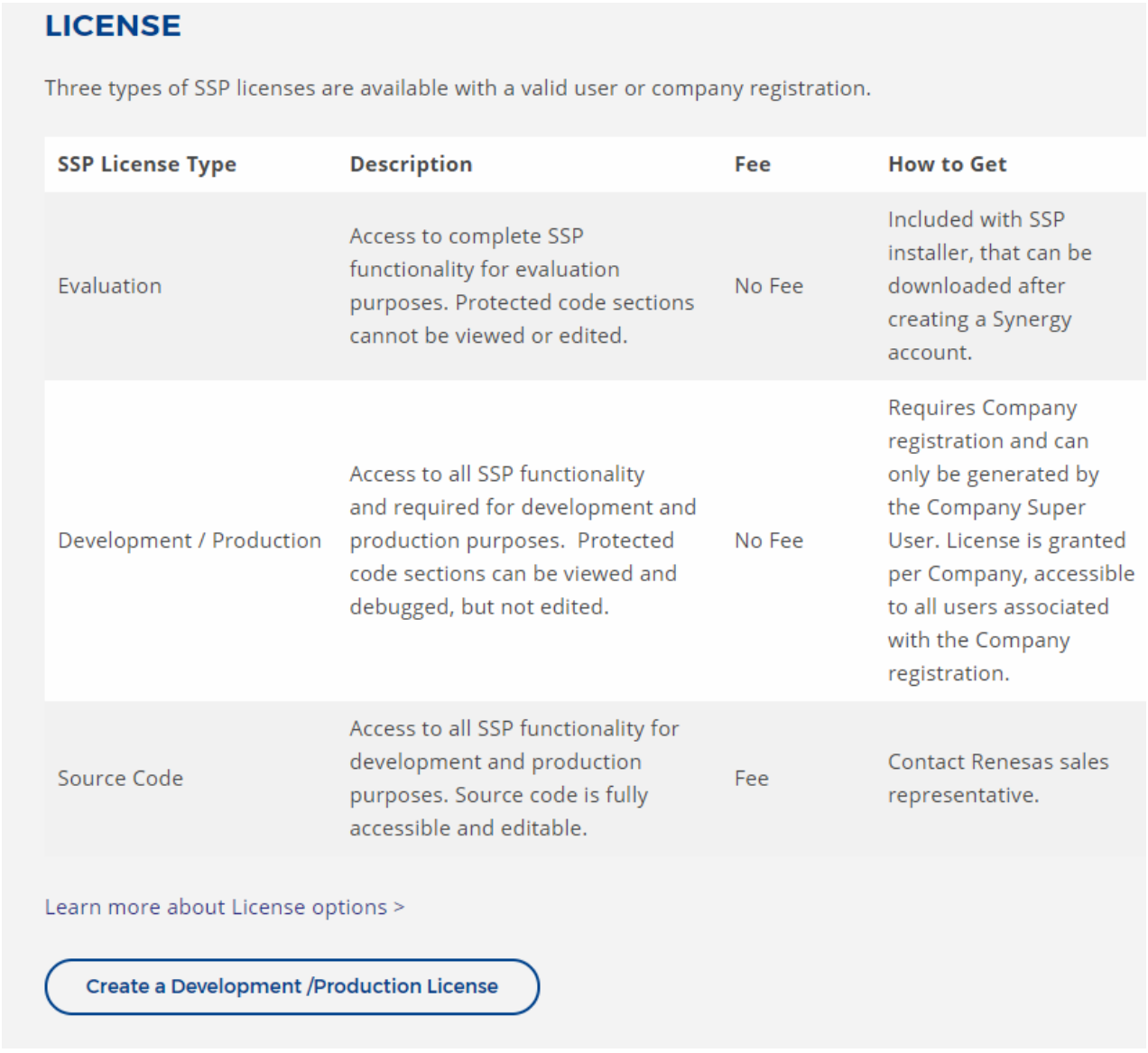
Note: The default installation folder for the SSP is **C:\Renesas\e2_studio**.

SSP documentation is available for download from the Synergy Software Package (SSP) page in Renesas Synergy Platform section, at https://www.renesas.com/synergy/software/ssp. Sign in to the MyRenesas account by using your existing MyRenesas or Synergy Gallery credentials, or by creating a new MyRenesas account.

Notes:

1. Users are required to generate and download a new Development and Production License Key file from Synergy Software Package (SSP) page in Renesas Synergy Platform section, on Renesas.com and apply it to your projects when upgrading to SSP v1.7.0. Using an older Development and Production License Key file generated/issued prior to SSP v1.7.0 will result in a build failure for all existing and new SSP v1.7.0 projects.
2. To generate and download a new License Key file, log on Renesas.com using your existing MyRenesas or Synergy Gallery credentials, or by creating a new MyRenesas account.

A new License Key file can be generated by your Company Super User by clicking the "*Create a Development/Production License*" link under the SSP section.



LICENSE

Three types of SSP licenses are available with a valid user or company registration.

SSP License Type	Description	Fee	How to Get
Evaluation	Access to complete SSP functionality for evaluation purposes. Protected code sections cannot be viewed or edited.	No Fee	Included with SSP installer, that can be downloaded after creating a Synergy account.
Development / Production	Access to all SSP functionality and required for development and production purposes. Protected code sections can be viewed and debugged, but not edited.	No Fee	Requires Company registration and can only be generated by the Company Super User. License is granted per Company, accessible to all users associated with the Company registration.
Source Code	Access to all SSP functionality for development and production purposes. Source code is fully accessible and editable.	Fee	Contact Renesas sales representative.

Learn more about License options >

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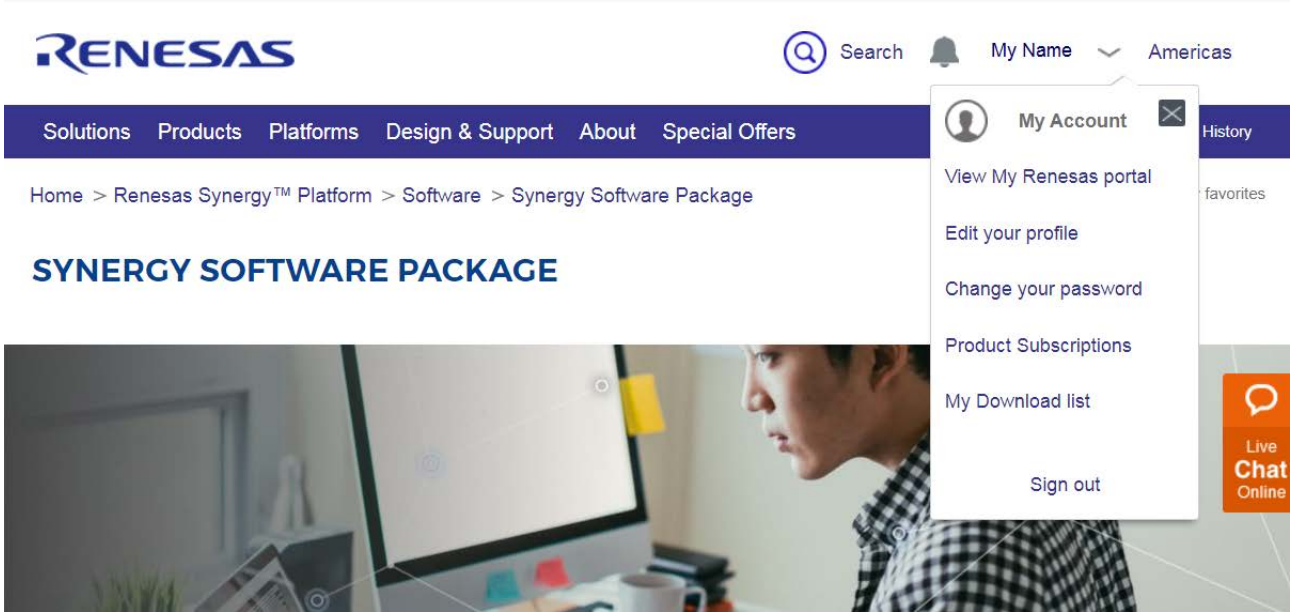
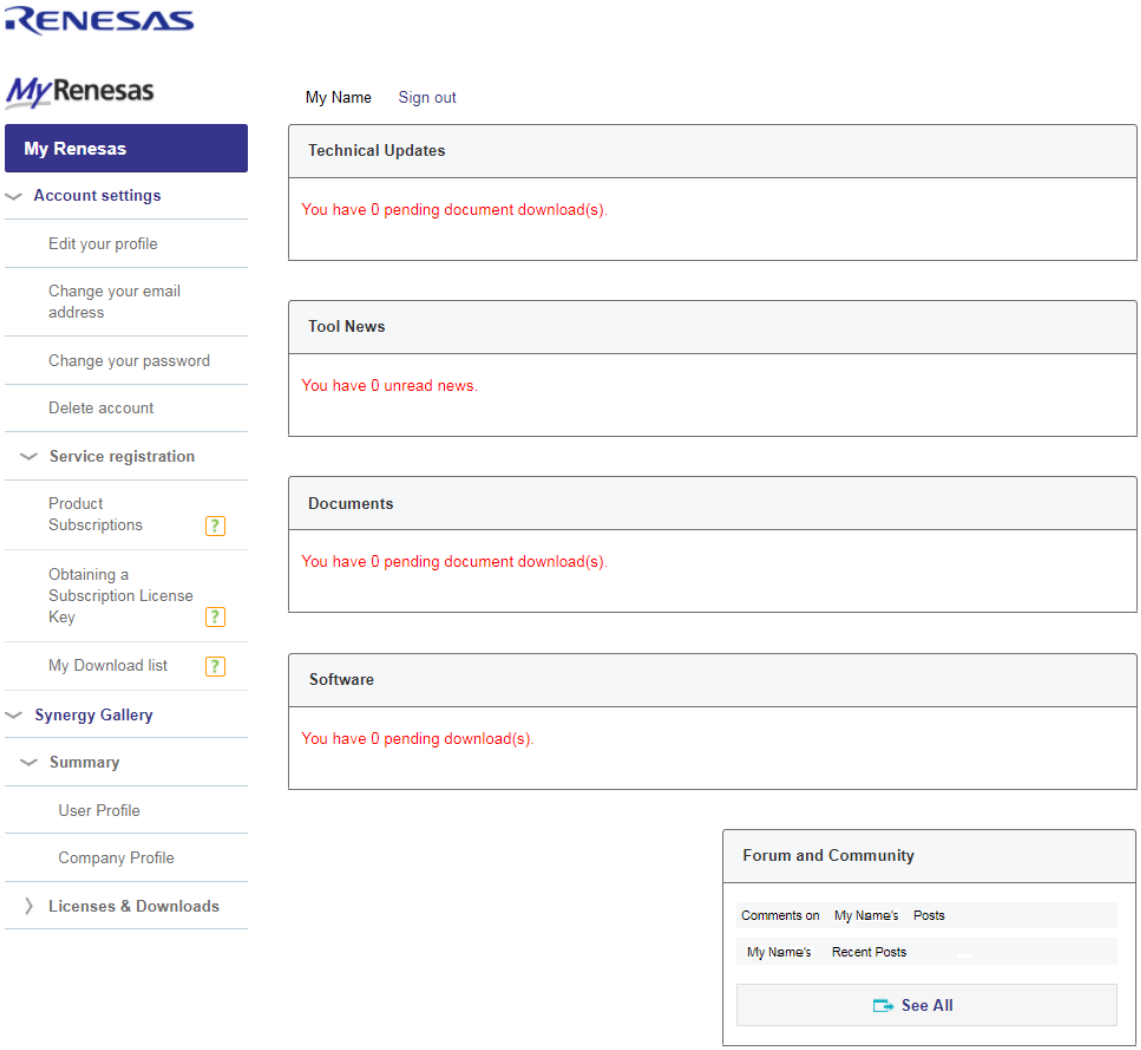
Once generated, the new License Key file can be downloaded by all users registered under that company account from the *Licenses and Downloads* section of *MyRenesas Portal* page. To access *MyRenesas Portal*, click the user name at the top of web page, then select ***View My Renesas Portal*** from the drop-down list as shown in the following screen captures.





6. Updates to SSP v1.7.0

SSP v1.7.0 is a qualified release for the new features and enhancements delivered as part of SSP v1.6.3. SSP v1.7.0 is being provided to facilitate customers requiring a completely qualified SSP release for the purpose of certification or production.

6.1 New or Updated Features

There are no new features in SSP v1.7.0.

6.2 Improvements in SSP v1.7.0

6.2.1 r_fmi

Issue ID: 15524

Updates have been made to the r_fmi module for SSP internal architectural improvements. These updates are not expected to have an impact on projects based on SSP.

In addition, due to the sensitive nature of the contents of the FMI (Factory MCU Information), in SSP v1.7.0 and all future SSP releases, the r_fmi module will be provided in protected source code format to prevent changes to the FMI module, which could potentially lead to adverse impact on the Synergy MCUs.

Due to the risks posed by changing the r_fmi module, all SSP releases made prior to SSP v1.7.0 are being withdrawn from Synergy Gallery. If an existing Synergy customer with an existing SSP Development and Production License generated prior to SSP v1.7.0 requires access to an older SSP or tools release, it will be made available upon request.

Applies to: All MCUs

7. Known Issues and Limitations in SSP v1.7.0

7.1 ISDE User Experience

Issue ID: 12826

If Synergy Configuration window is maximized in e^2 studio, the property window will not be updated.

Applies to: All MCUs

Workaround: Do not maximize the Synergy Configuration window before clicking on elements when editing the properties.

7.2 MCU Implementation/SW Architecture

Issue ID: 15277

P208, P209, P210, and P211 pins are not defined in the SSP `iodefine` file, and therefore cannot be accessed.

Applies to: S5D5 MCU Group

Workaround: None

7.3 NetX

Issue ID: 12951

Users will not be able to use TLS 1.0 for secure connection.

Applies to: S7G2, S5D9, S5D5, and S5D3 MCU Groups

Workaround: None

Issue ID: 13297

Web HTTP Client fails to reconnect with the server after the server has disconnected from the client. It returns error code 0x22, that is, socket is already bound.

Applies to: S7G2, S5D9, and S5D5 MCU Groups

Workaround: Access the internal HTTP client clean-up function executed when an error occurs. Use the following steps for implementation:

1. Provide prototype to the function in the C scope that you would like to use it in:
   `VOID _nx_web_http_client_error_exit(NX_WEB_HTTP_CLIENT *, UINT);`
2. Call `_nx_web_http_client_error_exit(p_http, timeout)` to force TLS termination and TCP disconnection and unbinding.
3. Now, the application is ready to call `nx_web_http_client_connect` or `nx_web_http_client_secure_connect` again. If the client is not in the ready state, it will perform `_nx_web_http_client_cleanup` (effectively resetting client state to ready/zero) before proceeding with a new connection.

Issue ID: 15088

NetX DHCP client fails to work if the DHCP server is sending messages on a UDP port number other than 67.

Applies to: NetX DHCP Client interface on all Synergy boards

Workaround: None

Issue ID: 15366

`nx_packet_release()` function always returns NX_PTR_ERROR instead of NX_UNDERLOW and NX_OVERFLOW even when the packet pointer overflows or underflows.

Applies to: S7G2, S5D9, S5D5, and S5D3 MCU Groups

Workaround: None

Issue ID: 15538

When using NetX/NetX Duo BSD projects with C++ compiler, the project fails with build error due to the unavailability of C++ macro in the `nx_bsd.h` or `nxd_bsd.h` file.

Applies to: All MCUs

Workaround: Disable Synergy builder in the `nx_bsd.h` file, and wrap all the function definitions with the following macro:

```
#ifdef __cplusplus
extern "C"
{
#endif
Function definitions
#ifdef __cplusplus
}
/* extern "C" */
#endif
```

Issue ID: 15549

When the ethernet interface is attached to a NetX Duo instance as a secondary interface and is detached multiple times, the ethernet driver does not release all the packets correctly and the packet pool will become depleted. This causes the application to fail.

Applies to: S7G2, S5D9, S5D5, and S5D3 MCU Groups

Workaround: None

7.4 nxd_mqtt_client

Issue ID: 15331

In the NetX Duo MQTT client using TLS, NX_WAIT_FOREVER is used when starting the TLS session in the function `_nxd_mqtt_client_connect()`. This could potentially cause the thread to hang.

Applies to: S7 and S5 MCU Series

Workaround: None

7.5 nxd_tls_secure

Issue ID: 14714

For ECC Cipher Suite with AES GCM Cipher algorithm, the output buffer size is defined as 2048 bytes.

If the incoming message is greater than 2048 bytes, the data transfer will fail.

Applies to: S5 and S7 MCU Series

Workaround 1:

Application should breakdown a large data buffer into 2K chunks.

Workaround 2:

- Define NX_CRYPTO_AES_OUTPUT_BUFFE_SIZE to 4096 in `sf_el_nx_crypto\nx_crypto_aes_sce.h`
- Increase the metadata buffer size for the application accordingly.

7.6 Pin Mapping Issues

Issue ID: 14452

The current driver uses AVCC0 as the reference voltage for internal ADC. When internal voltage measurement or VREFH0, VREFL0 is selected, pin conflict is observed in the tools and the driver does not support these features.

Applies to: S3 and S1 MCU Series

Workaround: None

7.7 r_adc

Issue ID: 15559

In the Synergy configuration tool, no warning or error is being displayed to resemble the error on the maximum allowed frequency for ADC in the S1JA MCU Group.

Applies to: S1JA MCU Group

Workaround: The user has to change PCLKD to the maximum supported frequency (32 MHz)

7.8 r_agt_input_capture

Issue ID: 15070

While capturing pulse width with AGT input capture, after a measurement completion, the counter and overflow value returned from callback are fine, but the same values read simultaneously with `lastCaptureGet` API are incorrect.

Applies to: All MCUs

Workaround: None

Issue ID: 15090

The agt_input_capture.xml sets the corresponding PCLKB value to PCLKB/8 or PCLKB/2 options. Therefore, the PCLKB/8 or PCLKB/2 selection is not reflected in the code.

Applies to: All MCUs

Workaround: After the user creates the agt input capture project, click **Generate Project Content** to generate the code specific to the config.xml properties, then go to **Project** > **Properties** > **Builders** and disable the Synergy builder. Then, go to Synergy generated `hal_data.c` file and change the `g_input_capture_extend.count_source` to AGT_INPUT_CAPTURE_CLOCK_PCLKB_DIV_2 or AGT_INPUT_CAPTURE_CLOCK_PCLKB_DIV_8, and build the project to get the expected source clock.

Issue ID: 15091

While initializing the AGT Input Capture using `open` API with source clock as AGTSCLK, (that is, sub-clock for AGT), if this sub-clock oscillator source clock is off, the capture will not happen (as there is no input clock), but the `open` API returns success.

Applies to: All MCUs

Workaround: Use the CGC API to activate the sub-clock as follows, before calling AGT Input Capture `open` API:

```
g_cgc.p_api->clockStart(CGC_CLOCK_SUBCLOCK,NULL);
```

Issue ID: 15130

In AGT Input Capture Event mode, if the pulse count is measured from an external hardware, the first callback is triggered in the expected time (corresponding to the input signal frequency), but the subsequent callbacks after that take more time, which is not correct. The captured values are correct but they are not triggered in expected times.

Applies to: All MCUs

Workaround: None

7.9 r_ctsu

Issue ID: 8731

In case of a hardware issue where the channel capacitance has an invalid value (due to board layout), the CTSU data acquisition fails. The code waits in a loop for the data, and does not return.

Applies to: All MCUs

Workaround: Make sure that the TSCAP has the recommended capacitor connected

7.10 r_dac8

Issue ID: 12261

The DAC8 output pin is not being configured when it is configured through ISDE.

Applies to: S1JA, S128, and S3A3 MCU Groups

Workaround: Configure the DAC8 output pin manually

7.11 r_gpt

Issue ID: 15553

`R_GPT_Reset` API fails to reset the GTCNT register in the GPT module.

Applies to: S124 MCU Group

Workaround: None

7.12 r_jpeg_decode

Issue ID: 14514

In the application with compiler GCC 7.2 optimization -O2, where encode and decode happen repeatedly, one after the other, the first iteration happens as expected, but from subsequent iterations, there are inconsistencies in the JPEG encoder's and decoder's output.

Applies to: S5D9 MCU Group

Workaround: For applications using both JPEG decode and encode repeatedly on GCC7.2, -O0 optimization has to be set to work effectively. Additionally, for JPEG encoder in the application, set the data types used in RGB to YCBCR conversion as double.

7.13 r_rspi

Issue ID: 15316

In SPI slave mode, SPI peripheral does not wait to become idle while performing write/read operations. As a result, data transfer will not happen properly when write/read APIs are called consecutively.

Applies to: All MCUs

Workaround: None

Issue ID: 15526

The RSPI module in an application can experience overrun error, if using DTC for data transfer, if the same application makes heavy use of DMAC.

Applies to: All MCUs

Workaround: None

Issue ID: 15337

The RSPI driver is supposed to drive the MOSI line (MISO in case of slave mode) to continuous high state while performing read operation. However, when DTC is used for the transfer MOSI (MISO in case of slave), the line may not always be at continuous high state.

Applies to: All MCUs

Workaround: Using RSPI read operation without DTC will drive MOSI line (MISO in case of slave) to continuous high state.

Issue ID: 15338

RSPI peripheral does not support the following conditions in slave mode:

When ‘Clock phase’ property is set to ‘Data sampling on odd edge, data variation on even edge’ (that is CPHA = 0) and Slave select input line is fixed at the active state, or continuous serial transfer (burst transfer) mode is enabled.

Applies to: All MCUs

Workaround: None

Issue ID: 15400

Incorrect data is being sent when RSPI write is called with a transfer bit width of 8 bits and the DTC transfer size is set to 2 bytes or 4 bytes. There is no problem if the DTC transfer size is set to 1 byte and RSPI write is called with bit width of either 8, 16, or 32 bits.

Applies to: All MCUs

Workaround: For 8-bit SPI operation, configure transfer size to 1 byte in DTC configuration.

7.14 r_rtc

Issue ID: 15376

Values read from RTC capture registers are incorrect.

Applies to: S124, S128, S3A1, S3A3, S3A6, and S3A7 MCU Groups

Workaround: None

7.15 r_sci_spi

Issue ID: 15574

The SCI SPI module in an application can experience overrun error if using DTC for data transfer if the same application makes heavy use of DMAC.

Applies to: All MCUs

Workaround: None

7.16 sf_block_media_qspi

Issue ID: 15219

In media type QSPI, in FileX on Block Media, while enabling the 'format media during initialization' property, the working media memory size should be equal to or greater than the block size of media in bytes, otherwise, it causes memory corruption.

Applies to: All MCUs

Workaround: None

7.17 sf_block_media_sdmmc

Issue ID: 15132

In an application with optimization -O2, while performing a repeated `fx_file_read` from an unaligned buffer, the `first fx_file_read` passes but the subsequent `fx_file_read` fails, and returns a FX_IO_ERROR.

Applies to: All MCUs

Workaround: Change the project optimization to -O0

7.18 sf_cellular

Issue ID: 14563

BG96 module fails to fallback from NB-IoT network to GSM or CATM1 cellular network SIM.

Applies to: Cellular Framework using BG96

Workaround: For GSM/CAT1 network SIM, the user should use either of the following network scan sequences:

- GSM > CAT-M1 > NB-IoT
- CAT-M1 > GSM > NB-IoT

Issue ID: 14566

Automatic time zone update disable functionality does not work. Even when the user disables automatic time zone update, the current updated time is received.

Applies to: CAT3, CAT1, and Quectel BG96 modules

Workaround: None

Issue ID: 15542

When the cellular interface is attached to a NetX Duo IP instance as a secondary interface and is detached, the cellular framework does not de-initialize since NX_LINK_INTERFACE_DETACH is not handled in the ethernet driver.

Applies to: Cellular modules on all MCUs

Workaround: None

7.19 sf_el_gx

Issue ID: 14094

The rotated texts using 1 bpp and 4 bpp font will not be rendered properly if D/AVE 2D rendering is used instead of software rendering.

Applies to: S7G2 and S5D9 MCU Groups

Workaround: Use 8 bpp font format for texts that need to be rotated in an application where D/AVE 2D rendering is used.

Issue ID: 15163

The GUIX application with rotation angle set to 90 or 270 degrees and software rendering enabled, will not be able to render an image properly on a non-square display. This may also corrupt the contents of the objects that are adjacent to the working frame buffer.

Applies to: A setup in which a non-square display is used.

Workaround: None

7.20 sf_el_lx_nor

Issue ID: 15230

If QSPI devices larger than 64 MB are used, QSPI sf_el_lx_nor framework reads data incorrectly for addresses greater than 64 MB.

Applies to: S7, S5, and S3 MCU Series

Workaround: If the QSPI device address in known, the user's application can call the `R_QSPI_BankSelect` API to change banks to access memory larger than 64 MB.

Issue ID: 15298

QSPI NOR write operation results in data corruption when the source and destination fall within the same QSPI NOR address space.

Applies to: All MCUs

Workaround: None

7.21 sf_el_nx

Issue ID: 15550

When the ethernet interface is attached to a NetX Duo IP instance as a secondary interface and is detached, the ethernet driver is not uninitialized since NX_LINK_INTERFACE_DETACH is not handled in the ethernet driver.

Applies to: S7G2, S5D9, S5D5, and S5D3 MCU Groups

Workaround: None

7.22 sf_el_tx

Issue ID: 13678

SF_CONTEXT_SAVE and SF_CONTEXT_RESTORE (in `bsp_common.h`) should only be defined if TX_ENABLE_EXECUTION_CHANGE_NOTIFY or TX_ENABLE_EVENT_TRACE is defined.

Applies to: All MCUs

Workaround: None

7.23 sf_el_ux

Issue ID: 13481

The USB host sends out a PING packet after receiving NAK or NYET handshake from the device. However, it also sends out a PING packet for ACK handshake, which is not expected behavior according to the USB 2.0 specification.

Applies to: All Synergy MCUs supporting USBX Host

Workaround: None

Issue ID: 13487

In USBX CDC-ACM device class, if the user disconnects the USB cable from the host PC while the terminal is in connected state, and then plugs the USB CDC cable, in this use case, if the user application checks the CDC line state parameter (DTR and RTS) immediately after the USB cable is plugged into the PC, it will reflect the previous state, which is incorrect.

Applies to: All MCUs

Workaround: First disconnect the terminal and then unplug the USB CDC cable from the host PC.

Issue ID: 15325

In USBX device class, when the host suspends the Synergy device controller, it receives a device state transition interrupt and wrongly calls `ux_device_stack_disconnect` when it receives a SUSPEND signal. As a result, it is forced to handle the SUSPEND signal as a disconnect.

Applies to: All MCUs

Workaround: None

Issue ID: 15335

Resume interrupt is not enabled in the USB DCD driver.

Applies to: All MCUs

Workaround: None

7.24 sf_i2c

Issue ID: 14618

With GCC 7.2 and optimization level -Og, sf_i2c `read` API (with sci_i2c driver) intermittently hangs when invoked with a timeout value of 0 instead of returning timeout error.

Applies to: All MCUs

Workaround:

- Use optimization level -O2.
- Instead of sci_i2c, use r_riic as the lower-level driver.

7.25 sf_memory_qspi_nor

Issue ID: 14137

If QSPI devices larger than 64 MB are used, QSPI (and LevelX) Block media drivers read data incorrectly for addresses greater than 64 MB.

Applies to: S7, S5, and S3 MCU Series

Workaround: If the QSPI device address is known, the user application can call the `R_QSPI_BankSelect` API to change banks to access memory sizes greater than 64 MB memory.

Issue ID: 15231

If QSPI devices larger than 64 MB are used, the memory QSPI NOR driver reads the data incorrectly for addresses greater than 64 MB.

Applies to: S7, S5, and S3 MCU Series

Workaround: If the QSPI device address is known, the user's application can call the `R_QSPI_BankSelect` API to change banks to access memory sizes greater than 64 MB memory.

7.26 sf_Wifi

Issue ID: 14314

If an ongoing WPS session gets terminated by a peer WiFi device, then the GT202 driver hangs. The GT202 Driver API for WPS is called by invoking WiFi framework APIs which use mutex. When GT202 driver hangs, it will cause WiFi WPS API to hang, resulting in WiFi APIs to return mutex error.

Applies to: All MCUs supported by GT202

Workaround: None

Issue ID: 15541

When the WiFi interface is attached to a NetX Duo IP instance as a secondary interface and detached, the WiFi framework does not de-initialize since NX_LINK_INTERFACE_DETACH is not handled in the framework.

Applies to: All MCUs

Workaround: None

7.27 SSP IAR Support

Issue ID: 12845

Cannot debug a program when selecting the option **Download and Debug** in EWSYN or **Debug** in e^2 studio the first time after setting an ID code in the project.

Applies to: All MCUs

Workaround: When the debug fails, select the option to **Debug without download** in EWSYN or **Debug** in e^2 studio again to successfully debug the program.

Issue ID: 13900

In some cases, the build fails with the error “Secure builder required” after migrating to a newer SSP version in EWSYN.

Applies to: All MCUs

Workaround: Select Project > Make (F7) after the issue occurs. The project should then build without errors.

7.28 SSP XMLs for ISDEs

Issue ID: 12857

Creating a project with a custom board pack might not reflect the customized values set for the properties in that custom board pack.

Applies to: All MCUs

Workaround: None

7.29 Synergy Tools

Issue ID: 11556

Synergy builder is excluded from the tool command pattern when changing the toolchain from IAR 7.x to IAR 8.x, which leads to a build error that the secure builder is required when trying to build the project after migrating.

Applies to: All MCUs

Workaround:

The following workaround can be used to migrate projects with IAR 7.x to IAR 8.x:

1. Add environment variable `SECURE_BUILD_COMMAND`: `${renesas.support.targetLoc:synergy-build} /isdebuild`
2. Update command line pattern IAR C/C++ Compiler for ARM setting if the following command is missing: `${SECURE_BUILD_COMMAND}`
3. Update command line pattern IAR C/C++ Assembler for ARM if the following command is missing: `${SECURE_BUILD_COMMAND}`

Issue ID: 12584

An error occurs when setting the watchpoint at certain addresses. Debug sessions cannot be started when these watchpoints with errors are still present.

Applies to: S5D9 MCU Group

Workaround: Remove the watchpoints from the breakpoints view and start the debug session.

Issue ID: 12925

When exporting the project, selecting the option for .tar format does not export the project in .tar format, but exports it in .zip format.

Applies to: Tools

Workaround: Edit the archive file name field by replacing the .zip with .tar, and the project will be exported in .tar format.

Issue ID: 14528

Deleting the `pincfg` file related to the old device after switching the device in the bsp tab leads to failure in generating project content with the new device.

Applies to: All MCUs

Workaround: None

Issue ID: 14747

When SSP 1.6.0 and a version later than SSP v1.6.0 are both installed, Developer assistance node in the project created with SSP 1.6.0 shows the function `wpsstart` which is not supported in SSP 1.6.0. Dragging and dropping the API to the source file will a show message about an unresolved method.

Applies to: Projects created with SSP v1.6.0 and using the RDS file created with later versions of SSP

Workaround: Do not drag and drop the `wpsstart` function from the Developer Assistant node in SSP v1.6.0.

Issue ID: 15203

When performing a clean build of a project in command line, the debug build configuration fails to be cleaned as the length of the "rm" command line has not adhered to the limit of console interface

Applies to: All MCUs

Workaround: None

Issue ID: 15536

In e^2 studio 7.4, only the threads that have a run count greater than 0 will be shown in the debug view. When one of the threads has a run count of 0, all the threads after that check do not populate in the debug view.

Applies to: All MCUs

Workaround: None

7.30 USBX

Issue ID: 15028

USBX HID class host is not sending repeated key events. When a keyboard key is pressed and held down, the key press event should be regenerated and sent out until the key is released.

Applies to: All MCUs

Workaround: None

Issue ID: 15551

USB Composite keyboard does not work when connected via USB 1.1 hub.

Applies to: S5 and S7 MCU Series

Workaround: None

7.31 USBX Device Development

Issue ID: 14091

In `ux_device_class_report_set` API, even though the function is successful, the status returns error.

Applies to: All MCUs

Workaround: None

8. Complete List of Modules Supported in this Release

These modules are available on the respective MCUs based on the following criteria:

- If the core functionality of the module has been tested and works on an MCU, even if it has known bugs, then the module is supported on the MCU.
- If the core functionality is broken or not tested on an MCU, then that module is not supported on the MCU.
- If a module is independent of the underlying MCU hardware or HAL drivers, and has been tested on a particular Synergy MCU, the following table indicates that this module is supported on all the Synergy MCUs that the underlying driver/framework/stack depend on have been tested.

8.1 BSP and Driver Modules Available in this Release

Module Name	SSP Feature	Supported Synergy MCU Groups
BSP	Board Support Package	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_acmphs	Analog Comparator High Speed	S1JA, S3A7, S5D9, S5D5, S5D3, S7G2
r_acmplp	Analog Comparator Low Power	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7
r_adc	A/D Converter	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_agt	Asynchronous General Purpose Timer	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_agt_input_capture	AGT Input Capture	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_analog_connect	Analog Connect	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_cac	Clock Frequency Accuracy Measurement Circuit	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_can	Controller Area Network	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_cgc	Clock Generation Circuit	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_crc	Cyclic Redundancy Check Calculator	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_ctsu	Capacitive Touch Sensing Unit	S124, S128, S3A7, S5D5, S5D9, S7G2
r_dac	Digital to Analog Converter	S124, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_dac8	8-bit Digital to Analog Converter	S128, S1JA, S3A3, S3A6
r_dmac	Direct Memory Access Controller	S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_doc	Data Operation Circuit	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_dtc	Data Transfer Controller	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_elc	Event Link Controller	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_flash_hp	Flash Memory, High Performance	S5D3, S5D5, S5D9, S7G2
r_flash_lp	Flash Memory, Low Power	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7
r_fmi	Factory Microcontroller Information	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_glcd	Graphics LCD Controller	S5D9, S7G2
r_gpt	General Purpose Timer	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2

Module Name	SSP Feature	Supported Synergy MCU Groups
r_gpt_input_capture	General Input Capture	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_icu	Interrupt Controller Unit	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_ioport	General Purpose I/O Ports	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_iwdt	Independent Watchdog Timer	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_jpeg_common	JPEG Common	S5D9, S7G2
r_jpeg_decode	JPEG Decode	S5D9, S7G2
r_jpeg_encode	JPEG Encode	S5D9, S7G2
r_kint	Keyboard Interrupt Interface	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_lpm†	Low Power Mode	S124, S3A7, S7G2
r_lpmv2_s1ja	Low Power Mode V2 for S1JA	S1JA
r_lpmv2_s124	Low Power Mode V2 for S124	S124
r_lpmv2_s128	Low Power Mode V2 for S128	S128
r_lpmv2_s3a1	Low Power Mode V2 for S3A1	S3A1
r_lpmv2_s3a3	Low Power Mode V2 for S3A3	S3A3
r_lpmv2_s3a6	Low Power Mode V2 for S3A6	S3A6
r_lpmv2_s3a7	Low Power Mode V2 for S3A7	S3A7
r_lpmv2_s5d3	Low Power Mode V2 for S5D3	S5D3
r_lpmv2_s5d5	Low Power Mode V2 for S5D5	S5D5
r_lpmv2_s5d9	Low Power Mode V2 for S5D9	S5D9
r_lpmv2_s7g2	Low Power Mode V2 for S7G2	S7G2
r_lvd	Low Voltage Detection Driver	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_opamp	Operational Amplifier	S128, S1JA, S3A1, S3A3, S3A6, S3A7
r_pdc	Parallel Data Capture Unit	S5D5, S7G2
r_qspi	Quad Serial Peripheral Interface	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
r_riic	IIC	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_riic_slave	IIC Slave	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_rspi	Serial Peripheral Interface	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_rtc	Real-time Clock	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_sci_i2c	Serial Communication Interface I2C	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_sci_spi	Serial Communication Interface SPI	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_sci_uart	Serial Communication Interface UART	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_sdadc	Sigma Delta ADC	S1JA
r_sdmmc	SDHI Driver for SDIO and SD/MMC Memory Devices	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
r_slcdc	Segment LCD Controller	S3A1, S3A3, S3A6, S3A7
r_ssi	(Inter-IC Sound) Interface [old: Serial Sound Interface] or r_i2s	S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2

Module Name	SSP Feature	Supported Synergy MCU Groups
r_wdt	Watchdog Timer	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_sce[#]	Cryptographic Library (HAL interfaces)	See table note on Cryptographic Functions

[#] **Cryptographic Functions**: Section 8.4 lists cryptographic functions available for each MCU in this release; these functions are accessible as part of r_sce/cryptographic library.

8.2 Framework Modules Supported in this Release

Module Name	SSP Feature	Supported Synergy MCU Groups
sf_adc_periodic	Periodic Sampling ADC	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_audio_playback	Audio Playback	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_audio_playback_hw_dac	Audio Playback HW DAC	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_audio_playback_hw_i2s	Audio Playback HW I2S	S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_audio_record_adc	Audio Record ADC	S124, S128, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_audio_record_i2s	Audio Record I2S	S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_ble_rl78g1d	BLE Framework	S124, S128, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_ble_rl78g1d_onboard_profile	BLE Framework Onboard Profiles	S124, S128, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_block_media_lx_nor	Block Media Interface for LevelX NOR	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
sf_block_media_qspi	Block Media Interface for QSPI	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
sf_block_media_ram	Block Media Interface for RAM	S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_block_media_sdmmc	Block Media Interface for SD Multi Media Card	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
sf_comms_telnet	Telnet Communications	S5D3, S5D5, S5D9, S7G2
sf_console	Console	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_el_fx	Synergy FileX interface	S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_el_gx	Synergy GUIX Interface	S5D9, S7G2
sf_el_lx_nor	Synergy LevelX NOR Interface	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
sf_el_nx	Synergy NetX Interface	S5D5, S5D9, S7G2
sf_el_nx_comms	Synergy NetX Communication Interface	S5D5, S5D9, S7G2
sf_el_ux	Synergy USBX Interface	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_el_ux_comms†	Synergy USBX Communication Interface	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_el_ux_comms_v2	Synergy USBX Communication Interface V2	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2

Module Name	SSP Feature	Supported Synergy MCU Groups
sf_external_irq	External Interrupt	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_i2c	I2C Framework	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_jpeg_decode	JPEG Decode	S5D9, S7G2
sf_memory_qspi_nor	Memory QSPI NOR	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
sf_message	Inter-Thread Messaging	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_power_profiles†	Power Mode Profile	S124, S3A7, S7G2
sf_power_profiles_v2	Power Mode Profile V2	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_spi	SPI Framework	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_tes_2d_drw	2D Drawing Engine Framework	S5D9, S7G2
sf_thread_monitor	Thread Monitor (Watchdog)	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_touch_ctsu	Capacitive Touch Sensing Unit	S124, S128, S3A7, S5D9, S7G2
sf_touch_ctsu_button	Capacitive Touch Sensing Unit Button	S124, S128, S3A7, S5D9, S7G2
sf_touch_ctsu_slider	Capacitive Touch Sensing Unit Slider	S124, S128, S3A7, S5D9, S7G2
sf_touch_panel_i2c	Touch Panel I^2C	S5D9, S7G2
sf_touch_panel_v2	Touch Panel Version 2	S5D9, S7G2
sf_uart_comms	UART Framework	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_wifi_gt202	Wi-Fi Framework	S124, S128, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_wifi_gt202_onchip	Wi-Fi framework on Chip Stack	S124, S128, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_cellular_catm1	Cellular Framework Quectel BG96 CATM1	S5D9, S7G2
sf_cellular_catm1_socket	Cellular Framework Quectel BG96 CATM1 Socket	S5D9, S7G2
sf_cellular_cat1	Cellular Framework Nimbelink CAT1	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
sf_cellular_cat1_socket	Cellular Framework Nimbelink CAT1 Socket	S128, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_cellular_cat3	Cellular Framework Nimbelink CAT3	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
sf_cellular_cat3_socket	Cellular Framework Nimbelink CAT3 Socket	S128, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_crypto#, ##	Cryptographic Framework	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_el_nx_crypto	Cryptographic Framework-Shim layer	S5D3, S5D5, S5D9, S7G2

Cryptographic Functions: Section 8.4 lists cryptographic functions available for each MCU in this release; these functions are accessible as part of r_sce/cryptographic library.

Framework Interfaces for Cryptographic Functions (sf_crypto) available for this release include: HASH, TRNG, and Key Generation (RSA and AES).

† Indicates a module that is deprecated starting with SSP v1.3.0 and all subsequent versions. Deprecated modules will only be available to maintain compatibility with existing projects that may be using them. It is highly recommended that new projects use the recommended replacements and not use deprecated modules. For details, see the *SSP User's Manual*.

8.3 Third-Party Modules Supported in this Release

Module Name	SSP Feature	Supported Synergy MCU Groups
fx	FileX	S124, S3A3, S3A6, S3A7, S5D9, S7G2
gx	GUIX	S5D9, S7G2
nx	NetX	S5D9, S7G2
nx_auto_ip	NetX Auto IP	S5D9*, S7G2
nx_bsd	NetX BSD	S5D9*, S7G2
nx_dhcp_client	NetX DHCP Client	S5D9*, S7G2
nx_dhcp_server	NetX DHCP Server	S5D9*,
nx_dns_client	NetX DNS Client	S5D9*, S7G2
nx_ftp_client	NetX FTP Client	S5D9*, S7G2
nx_ftp_server	NetX FTP Server	S5D9*, S7G2
nx_http_client	NetX HTTP Client	S5D9*, S7G2
nx_http_server	NetX HTTP Server	S5D9*, S7G2
nx_pop3	NetX POP3	S5D9*, S7G2
nx_ppp	NetX PPP	S5D9*, S7G2*
nx_smtp_client	NetX SMTP Client	S5D9*, S7G2
nx_snmp	NetX SNMP	S5D3*, S5D5*, S5D9*, S7G2
nx_sntp_client	NetX SNTP Client	S5D9*, S7G2
nx_telnet_client	NetX Telnet Client	S5D9*, S7G2
nx_telnet_server	NetX Telnet Server	S5D9*, S7G2
nx_tftp_client	NetX TFTP Client	S5D9*, S7G2
nx_tftp_server	NetX TFTP Server	S5D9*, S7G2
nxd	NetX Duo Stack	S5D9, S7G2
nxd_auto_ip	NetX Duo Auto IP	S5D9*, S7G2
nxd_bsd	NetX Duo BSD	S5D9*, S7G2
nxd_dhcp	NetX Duo DHCP IPv4 Client	S5D9*, S7G2
nxd_dhcp	NetX Duo DHCP IPv6 Client	S5D9*, S7G2
nxd_dhcp_server	NetX Duo DHCP IPv4 Server	S5D9*, S7G2
nxd_dhcp_server	NetX Duo DHCP IPv6 Server	S5D9*, S7G2
nxd_dns	NetX Duo DNS Client	S5D9*, S7G2
nxd_ftp_client	NetX Duo FTP Client	S5D9*, S7G2
nxd_ftp_server	NetX Duo FTP Server	S5D9*, S7G2
nxd_http_client	NetX Duo HTTP Client	S5D9*, S7G2
nxd_http_server	NetX Duo HTTP Server	S5D9*, S7G2
nxd_nat	NetX Duo NAT	S5D9*, S7G2
nxd_pop3	NetX Duo POP3	S5D9*, S7G2
nxd_ppp	NetX Duo PPP	S5D9*, S7G2*
nxd_smtp_client	NetX Duo SMTP Client	S5D9*, S7G2
nxd_snmp	NetX Duo SNMP	S5D3*, S5D5*, S5D9*, S7G2
nxd_sntp_client	NetX Duo SNTP Client	S5D9*, S7G2
nxd_telnet_client	NetX Duo Telnet Client	S5D9*, S7G2
nxd_telnet_server	NetX Duo Telnet Server	S5D9*, S7G2
nxd_tftp_client	NetX Duo TFTP Client	S5D9*, S7G2
nxd_tftp_server	NetX Duo TFTP Server	S5D9*, S7G2

Module Name	SSP Feature	Supported Synergy MCU Groups
nxd_mqtt_client	NetX Duo MQTT Client	S5D3, S5D5, S5D9, S7G2
nxd_tls_secure	NetX Duo TLS Secure	S5D3, S5D5, S5D9, S7G2
nxd_web_http_client	NetX Duo Web HTTP1.1 Client	S5D5*, S5D9, S7G2
	NetX Duo Web HTTPS Client	S5D5, S5D9, S7G2
nxd_web_http_server	NetX Duo Web HTTP1.1 Server	S5D9, S7G2
	NetX Duo Web HTTPS Server	S5D9, S7G2
Tx	ThreadX	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
Lx_nor	LevelX NOR	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
ux_device_class_storage	USBX Device Class Mass Storage	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
ux_device_class_hid	USBX Device Class HID	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
ux_device_class_cdc_acm	USBX Device Class CDC-ACM	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
ux_host_class_cdc_acm	USBX Host Class CDC-ACM	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
ux_host_class_hid	USBX Host Class HID	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
ux_host_class_hub	USBX Host HUB	S5D3, S5D5, S5D9, S7G2
ux_host_class_storage	USBX Host Class Mass Storage	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
ux_host_class_video	USBX Host Video class	S5D9, S7G2

* NetX and NetX Duo Applications are MCU-independent application layer protocols dependent on the NetX and Ethernet drivers. All MCUs on which NetX has been tested and verified support these protocols.

8.4 Cryptographic Functions for Each MCU Supported in this Release

Function	S5D3, S5D5, S5D9, S7G2	S3A1, S3A3, S3A6, S3A7	S124, S128, S1JA
TRNG	Generate and read random number	Generate and read random number	Generate and read random number
AES	Encryption, decryption, Key Generation - wrapped keys	Encryption, decryption, Key Generation - wrapped keys	Encryption, decryption
AES Key Size	128-bit, 192-bit, 256-bit	128-bit, 256-bit	128-bit, 256-bit
AES Key Type	Plain text / raw key, wrapped key	Plain text / raw key, wrapped key	Plain text / raw key
AES Chaining Modes	ECB, CBC, CTR, GCM, XTS† †	ECB, CBC, CTR, GCM, XTS	ECB, CBC, CTR
ARC4	Encryption, decryption	NA	NA
TDES	Encryption, decryption	NA	NA
TDES Key Size	192-bit	NA	NA
TDES Chaining Modes	ECB, CBC, CTR	NA	NA
RSA	Signature Generation, Signature Verification, Public-key Encryption, Private-key Decryption, Key Generation - plain text and wrapped keys	NA	NA

Function	S5D3, S5D5, S5D9, S7G2	S3A1, S3A3, S3A6, S3A7	S124, S128, S1JA
RSA Key Size	1024-bit, 2048-bit	NA	NA
RSA Key Type	Plain text / raw key, Wrapped key	NA	NA
Key Installation	AES, ECC, RSA keys	AES keys	NA
ECC	Key Generation – plain text and wrapped keys, Scalar Multiplication, ECDSA – Signature Generation, ECDSA – Signature Verification	NA	NA
ECC Key Size (in bits)	192-bit, 224-bit, 256-bit, and 384-bit	NA	NA
ECC Key Type	Plain text / raw keys and wrapped keys	NA	NA
DSA	Signature Generation, Signature Verification	NA	NA
DSA Key Size	(1024, 160)-bit, (2048, 224)-bit, (2048, 256)-bit	NA	NA
HASH	SHA1, SHA224, SHA256, MD5	NA	NA

†† XTS is supported for 128-bit and 256-bit keys only.

8.5 Experimental Modules Supported in this Release

Modules that have not been tested on the MCUs have been classified as experimental modules and are listed in the following table. These experimental modules are currently not supported by Synergy Configuration tools and use of these modules in customer projects is not supported by Renesas at this time.

Experimental Modules		
Module Name	**SSP Feature**	**Supported Synergy MCU Groups**
ux_device_class_cdc_ecm	USBX Device Class CDC-ECM	S124, S3A3, S3A7, S5D9, S7G2
ux_device_class_rndis	USBX Device Class RNDIS	S124, S3A3, S3A7, S5D9, S7G2
ux_host_class_gser	USBX Host Class Generic Serial	S3A3, S3A7, S5D9, S7G2
ux_host_class_printer	USBX Host Class Printer	S3A3, S3A7, S5D9, S7G2
ux_host_class_prolific	USBX Host Class Prolific	S3A3, S3A7, S5D9, S7G2
ux_host_class_swar	USBX Host Class Swar	S3A3, S3A7, S5D9, S7G2
ux_network_driver	USBX Network Driver	S124, S3A3, S3A7, S5D9, S7G2

9. Additional Technical Notes

- Subscribe to the Synergy Technical Bulletin Board to receive the latest technical news and notifications about new features, known issues, workarounds, and release announcements. To subscribe, visit www.renesasrulz.com/synergy/synergy_tech_notes/f/214.aspx. Sign in to Renesas Rulz, and press **Email Subscribe to this forum**.
- Additional technical information, including informative papers and articles on SSP and Synergy can be found at Synergy Knowledge Base, www.renesas.com/synergy/knowledgebase.

Website and Support

Visit the following vanity URLs to learn about key elements of the Synergy Platform, download components and related documentation, and get support.

Synergy Software	www.renesas.com/synergy/software
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Revision History

Rev.	Date	Description	
		Page	Summary
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