Release Note

# SSP v1.7.8

Release Note

## Renesas Synergy™ Platform
## Synergy Software
## Synergy Software Package



Renesas Electronics
www.renesas.com

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Renesas Synergy™ Platform

# SSP v1.7.8 Release Note

## Contents

## 1. Introduction

This document describes the release notes for **Synergy Software Package (SSP) version 1.7.8**.

## 2. Release Information

| | |
|---|---|
| SSP Release Version | v1.7.8 |
| Release Date | Jun 19, 2020 |

The intended audience for this release note is Renesas Synergy™ customers, prospective customers, partners, and support staff. This release note describes the fixed issues and known issues in SSP v1.7.8.

## 3. Synergy MCU Groups Supported

MCU Groups: S7G2, S5D9, S5D5, S5D3, S3A7, S3A6, S3A3, S3A1, S128, S124, and S1JA.

## 4. Software Tools and Hardware Kits Supported with this SSP Release

| Tool | Version | Description |
|---|---|---|
| e$^2$ studio | 7.5.1 | Software development and debugging tool.<br>Link: www.renesas.com/synergy/tools |
| IAR Embedded Workbench® for Renesas Synergy™ | 8.23.3 | Software development environment and debugging tool.<br>Link: www.renesas.com/synergy/tools |
| SSC | 7.5.1 | Synergy Standalone Configurator.<br>Used in combination with IAR EW for Synergy.<br>Link: www.renesas.com/synergy/tools |
| GNU Arm Compiler | 7.2.1 and 4.9.3 | Both versions of GNU Arm® compilers are supported with SSP v1.7.8<br>Note: GCC 4.9.3 does not support S1JA MCU Group. |
| IAR Compiler | 8.23.3 | IAR Arm® compiler toolchain |
| PE-HMI1 | 2.0 | Product Example (PE) for Human Machine Interface to evaluate Renesas Synergy™ S7G2 MCU Group |
| DK-S7G2 | 4.1 | Development Kit for Renesas Synergy™ S7G2 MCU Group |
| SK-S7G2 | 3.3 | Starter Kit for Renesas Synergy™ S7G2 MCU Group |
| PK-S5D9 | 1.0 | Promotion Kit for Renesas Synergy™ S5D9 MCU Group |
| TB-S5D5 | 1.1 | Target Board Kit for Renesas Synergy™ S5D5 MCU Group |
| TB-S5D3 | 1.0 | Target Board Kit for Renesas Synergy™ S5D3 MCU Group |
| DK-S3A7 | 2.0 | Development Kit for Renesas Synergy™ S3A7 MCU Group |
| TB-S3A6 | 1.0 | Target Board Kit for Renesas Synergy™ S3A6 MCU Group |
| TB-S3A3 | 1.0 | Target Board Kit for Renesas Synergy™ S3A3 MCU Group |
| TB-S3A1 | 1.0 | Target Board Kit for Renesas Synergy™ S3A1 MCU Group |
| DK-S128 | 1.1 | Development Kit for Renesas Synergy™ S128 MCU Group |
| DK-S124 | 3.1 | Development Kit for Renesas Synergy™ S124 MCU Group |
| TB-S1JA | 1.2 | Target Board Kit for Renesas Synergy™ S1JA MCU Group |
| J-Link Software | 6.34e | SEGGER J-Link® debug probe is the quasi standard for Arm® Cortex®-M based MCUs |

## 4.1 Version Information for Third-Party Products

| Component | Version in SSP v1.7.8 |
|---|---|
| ThreadX® | 5.9 |
| NetX™ | 5.12 SP1 |
| NetX Duo™ | 5.12 SP1 |
| NetX Application bundle | 5.12 SP1 |
| NetX Duo Application bundle (MQTT, SNMP, Web HTTP) | 5.12 SP1 |
| USBX™ Host | 5.9 SP1 |
| USBX™ Device | 5.9 SP1 |
| FileX® (exFAT) | 5.6 SP1 (private release 1.6.1-b.2) |
| GUIX™ | 5.6 SP1 |
| LevelX | 5.6 |
| TraceX® | 5.2.0 |
| GUIX Studio™ | 5.6.1.0 |
| NetX Secure | 5.12 SP1 |
| NetX Duo Secure | 5.12 SP1 |
| TES D/AVE 2D | 3.17 |

## 5. SSP Release Package and Installation Information

Before installing SSP standalone installer, ensure that the following items are installed on your PC:

- **Renesas e² studio ISDE v7.5.1** (download and install the e² studio Installer from the Renesas website at www.renesas.com/synergy/software)
- **GNU Arm® Compiler** (included with Renesas e² studio ISDE v7.5.1)

To install the SSP, follow these steps:

1. Download the following items for the SSP Release from www.renesas.com/synergy/software:
   - **SSP_Distribution_1.7.8.zip** (SSP Package Installer, including SSP Package)
   - **Renesas Synergy Software Package (SSP) v1.7.8 Release Note**.
2. Unzip the package and run the **SSP_Distribution_1.7.8.exe** installer.
3. Install the SSP in the root folder of a compatible e² studio installation.

Note: The default installation folder for the SSP is **C:\Renesas\e2_studio**.

SSP documentation is available for download from the Synergy Software Package (SSP) page in Renesas Synergy Platform section, at www.renesas.com/synergy/ssp. Sign in to the MyRenesas account by using your existing MyRenesas or Synergy Gallery credentials, or by creating a new MyRenesas account.

# 6. Changes from SSP v1.7.5 to SSP v1.7.8

This section includes a list of issues fixed in SSP v1.7.8 release.

## 6.1 Issues Fixed in SSP v1.7.8

### 6.1.1 BSP for SSP Supported Platforms

**Issue ID**: 15739

Changed .data.* to *(.data*) and the `data_flash_symbol` in GCC linker script to `dflash` symbol. This may break compatibility for existing projects using `data_flash_symbol`.

To prevent compatibility issues, any projects using BSP_PLACE_IN_SECTION (".data_flash") or BSP_PLACE_IN_SECTION_V2 (".data_flash") should update to use BSP_PLACE_IN_SECTION (".dflash") or BSP_PLACE_IN_SECTION_V2 (".dflash") respectively,

**Applies to**: All MCUs

**Issue ID**: 15902

Data flash is now enabled for S1 and S3 parts in the BSP initialization.

**Applies to**: S3 and S1 MCU Series

**Issue ID**: 15903

The status of pins PA02 and PA03 is now restored after reading the board version from EEPROM in the BSP.

**Applies to**: S7G2 MCU Group

### 6.1.2 GUIX Studio

**Issue ID**: 15600

The GUIX Studio crashes sometimes if the **Reverse Byte Order** option is enabled when 2D Drawing Engine enabled in GUIX Studio. This issue is now fixed in GUIX studio 5.6.1.0.

**Applies to**: GUIX Studio

**Issue ID**: 15855

Synergy specific license file (GUIX_Studio.tag) is now included in the same directory as the GUIX Studio installer to install GUIX Studio with Synergy specific license.

**Applies to**: All MCUs

**Issue ID**: 15988

When GUIX Studio is used to export the resources to a binary file with compressed pixelmap output format, the output image is not displayed properly on the board.

This issue is fixed as part of GUIX Studio 5.6.1.0.

**Applies to**: GUIX Studio 5.6.1.0

### 6.1.3 NetX

**Issue ID**: 13297

Web HTTP client fails to reconnect with the server after the server has disconnected with the client. It returns error code 0x22, that is, socket is already bound. With the fix in NetX Duo 5.12 SP1, the client can successfully reconnect to the server multiple times.

**Applies to**: S7G2, S5D9, and S5D5 MCU Groups

**Issue ID**: 14484

When the nx_web_http_server function `nx_web_http_server_type_get()`is invoked with resource name ending with '/', the function returns a pointer to MIME string instead of the status code. With the fix in NetX Duo 5.12 SP1, the function `nx_web_http_server_type_get()`returns the status code.

**Applies to**: S7G2, S5D9, and S5D5 MCU Groups

**Issue ID**: 15218

When multiple network interfaces are used in an application, due to improper initialization in `nx_ip_thread_entry.c` file, bus fault is observed with compiler optimizations -O0,-O2 and -O3. This issue is fixed with the NetX 5.12SP1 update.

**Applies to**: S7G2, S5D9, S5D5, and S5D3 MCU Groups

**Issue ID**: 15366

With the NetX 5.12 SP1 update, `nx_packet_release()` function has been modified to return NX_OVERFLOW and NX_UNDERLOW when a pointer overflow/underflow occurs respectively instead of NX_PTR_ERROR.

**Applies to**: S7G2, S5D9, S5D5, and S5D3 MCU Groups

**Issue ID**: 15769

When using PPP on NetX or PPP on the cellular framework with PAP/CHAP authentication, PPP discards the PAP authentication requests when the username or password length is zero. This issue is fixed with EL 5.12 SP1 pack. Check for NULL username and password removed.

**Applies to**: All MCUs

### 6.1.4 nxd_mqtt_client

**Issue ID**: 15961

MQTT client connection is terminated when large messages are received from the server. This issue is fixed with the NetX Duo 5.12SP1 update.

**Applies to**: S7 and S5 MCU Series

### 6.1.5 nxd_tls_secure

**Issue ID**: 15825

When making an HTTPS connection to a server implemented on a Synergy MCU from a PC running Windows® 7 professional 64-bit and the Chrome browser, Chrome was sending a two-byte alert message to the server in plain text after the connection has switched to encrypted mode if the server is using a self-signed certificate. This operation causes the server to crash with a hard fault when NetX Secure attempts to interpret the plain text alert message as an encrypted message. This issue is now fixed with NetX Duo 5.12 SP1.

**Applies to**: All MCUs

**Issue ID**: 15859

- TLS v1.1 has been deprecated from SSP and will be obsolete starting from the next SSP release. Users are advised to upgrade their projects to use TLS v1.2 instead.
- TLS v1.1 will be excluded from SSP releases made after May 2021.
- TLS v1.1 has known security vulnerabilities and users are strongly advised to upgrade to TLS v1.2.

**Applies to**: All MCUs

### 6.1.6 r_adc

**Issue ID:** 15559

In the Synergy configuration tool, no warning or error is being displayed to resemble the error on the maximum allowed frequency for ADC in the S1JA MCU. This is fixed by updating the constraint for ADC and by adding the maximum ADC conversion clock for all MCUs in XML.

**Applies to**: S1JA MCU Group

**Issue ID:** 15803

`Calibration` API was called before choosing ADC internal reference voltage, which lead to a wrong calibrated reference value .This issue was observed only for internal voltage since, by default, the ADC reference voltage was VREFH0.

This issue is now resolved by setting the ADC internal reference voltage before calling the calibration routine.

**Applies to**: S1JA MCU Group

**Issue ID**: 15861

The analog input channels for channel-10 seems to not be detected with the FMI data calculation. An error is returned for R7FS3A6783A01CNF. However, for 100 pin CFP (R7FS3A6783A01CFP), the error is not observed.

This issue has been fixed by correcting the data stored in the FMI table for ADANSA0 register of R7FS3A6783A01CNF MCU.

**Applies to**: R7FS3A6783A01CNF MCU

### 6.1.7 r_agt

**Issue ID**: 15876

When AGT channel 0 is configured with **Count Source** set to **AGT0 Underflow**, recursion occurs between functions `agt_source_freq_get` and `agt_clock_frequency_get` and eventually hits NMI_Handler. With the fix, the driver returns an error to the user indicating the invalid use case.

**Applies to**: All MCUs

**Issue ID**:15877

In AGT HAL driver, when the timer is reset, the counter is initialized with the timer period. Due to this, the timer generated pulse width is increased by one source clock width. This issue was fixed by setting the counter to a period value -1 in the reset function.

**Applies to**: All MCUs

### 6.1.8 r_flash_hp

**Issue ID**: 15668

Optimization of hardware functions in flash_hp is taken off to avoid the misalignment in sequence of execution to register write due to optimization enabled for GCC

**Applies to**: All MCUs

### 6.1.9 r_pdc

**Issue ID**: 15746

DMAC interrupt priority is not correctly set up in R_PDC HAL driver. Value of the DMAC interrupt priority is taken as a random value in memory, which may lead to getting the same priority as **pendsv_handler**. Then, if the system has a chance to enter **pendsv_handler** for thread scheduling, it will no longer get out and the system will stay in the loop permanently.

This issue is now fixed by configuring the DMAC interrupt priority correctly in PDC HAL driver.

**Applies to**: S7G2 and S5D5 MCU Group

### 6.1.10 r_qspi

**Issue ID**: 15708

1. In N25Q256A, read/write operation of a non-volatile register was leading to wrong results. This is now addressed and reading and writing the non-volatile register gives the desired data as the LSB is read/written first and MSB later.

2. In MX25L12835F, volatile and non-volatile configuration registers cannot be accessed properly due to wrong commands. This is addressed and read/write non-volatile register commands are changed as per the datasheet.

**Applies to**: S7G2 MCU Group

### 6.1.11 r_riic

**Issue ID**: 15884

In `r_riic` driver, when an extra clock cycle is provided to reset the I2C bus, CLO bit should be cleared automatically. If CLO bit is not cleared automatically, the I2C bus is trapped in a loop waiting for the CLO bit to be cleared. Hence, to break the loop, a timeout mechanism is implemented.

**Applies to**: All MCUs

### 6.1.12 sf_audio_playback

**Issue ID**: 15804

After the `sf_audio_playback_hw_dac` is initialized to play an audio tone with the `open()` API, and before playing the audio tone with `start()` and `play()` APIs, no audio tone is played as expected, but a SF_AUDIO_PLAYBACK_HW_EVENT_PLAYBACK_COMPLETE event is received, indicating that the playback is complete. This issue has now been fixed.

**Applies to**: All MCUs

### 6.1.13 sf_cellular

**Issue ID**: 14563

BG96 module was failing to fallback from NBIoT network to GSM or CATM1 network SIM. It means GSM network SIM was not getting registered with GSM network if the Network Scan Sequence is set to one of the following:

NBIoT->GSM->CATM1

CATM1->NBIoT->GSM

NBIoT->CATM1->GSM

CATM1 network SIM was not getting registered with CATM1 network if the Network Scan Sequence is set to one of the following:

NBIoT->GSM->CATM1

GSM->NBIoT->CATM1

NBIoT->CATM1->GSM

This issue is fixed by increasing retry count to 255 for fallback from NBIoT network to GSM or CATM1 cellular network SIM in BG96 module.

**Applies to**: Cellular Framework using BG96

**Issue ID**: 15543

In Cellular Framework, the `sf_cellular_deinit()` function was deleting the PPP without stopping the PPP instance, thus not terminating the PPP correctly. This issue has now been fixed.

**Applies to**: Cellular modules on all MCUs

### 6.1.14 sf_el_lx_nor

**Issue ID**: 15230

If QSPI devices larger than 64 MB are used, QSPI memory QSPI NOR driver reads data incorrectly for addresses > 64 MB. This issue has been fixed by using `R_QSPI_BankSelect` API to change banks to access memory size more than 64 MB.

**Applies to**: S7, S5, and S3 MCU Series

### 6.1.15 sf_el_nx

**Issue ID**: 15758

Functions `bsp_ethernet_phy_init ()` and `nx_ip_status_check()` for NX_IP_LINK_ENABLED were returning success even when no PHY hardware is present. This issue has now been fixed.

**Applies to**: S7G2, S5D9, and S5D5 MCU Groups

### 6.1.16 sf_el_tx

**Issue ID**: 15615

Applications trying to restart a thread after `tx_thread_terminate`/`tx_thread_reset`/`tx_thread_resume` call have to use `tx_semaphore_put (&g_ssp_common_initialized_semaphore)` before restarting.

**Applies to**: All MCUs

### 6.1.17 sf_el_ux

**Issue ID**: 13487

Earlier, in the USBX CDC-ACM device class, if the user disconnected the USB cable from the PC host while the terminal is in connected state, and then plugged the USB CDC cable, if the user application checked the CDC line state parameter (DTR and RTS) immediately after the USB cable was plugged into the PC, it reflected the previous state, which is wrong. This issue is now fixed as part of the USBX 5.9 SP1 stack.

**Applies to**: All MCUs

**Issue ID**: 15370

The `ux_host_class_printer_status_get` function did not return correct status. This has now been fixed and the function returns the correct status.

**Applies to**: S7G2 and S5D9 MCU Groups

**Issue ID**: 15801

When an outgoing USB (bulk-in) transfer request is aborted, the next call to `ux_device_stack_transfer_request()` hangs up waiting for the `INBUFM` flag to clear.

Now, ACLRM bit is used for clearing the FIFO buffers resulting in the `INBUFM` flag getting cleared.

**Applies to**: All MCUs

### 6.1.18 sf_memory_qspi_nor

**Issue ID**: 15231

If QSPI devices larger than 64 MB are used, QSPI memory QSPI NOR driver reads data incorrectly for addresses > 64 MB. This issue has been fixed by using `R_QSPI_BankSelect` API to change banks to access memory size more than 64 MB.

**Applies to**: S7, S5, and S3 MCU Series

### 6.1.19 Synergy Tools

**Issue ID**: 14528

When switching the device and deleting the `pincfg` file related to an old device, the project generation still holds a reference to the deleted `pincfg` file and fails to generate project content. The tool now updates the `configuration.xml` file when the pin configuration file is deleted to fix the issue.

**Applies to**: All MCUs

### 6.1.20 USBX

**Issue ID**: 8505

The USBX Device Users Guide has been updated with error code UX_TRANSFER_BUFFER_OVERFLOW to indicate buffer overflow error.

**Applies to**: All MCUs

**Issue ID**: 14091

Earlier, `ux_device_class_hid_report_set` API always returned error, even though the HID device successfully received an event from the host. This issue is now fixed as part of the USBX 5.9 SP1 stack.

**Applies to**: All MCUs

**Issue ID**: 15381

The `ux_host_class_hid_idle_set` API information is now documented in the USBX Host Stack User Guide.

**Applies to**: All MCUs

**Issue ID**: 15814

With the update to the **Get/Set** feature in Express Logic code, the **GetReport** transfer failing issue is fixed. Additionally, support to configure callback function from XML is added.

**Applies to**: All MCUs

**Issue ID**: 15834

In USBX device class HID application, `device event notification callback` function is required for various device event notifications.

If this callback function is not configured in the configurator, the framework disconnects the device upon receiving the suspend signal from the host.

Therefore, to pass this **Suspend/Resume** compliance test, the user needs to configure the `device event notification callback` in the configurator.

**Applies to**: All MCUs

**Issue ID**: 15872

Debounce logic is implemented according to USB specifications in the USB host. This is to ensure stabilization of the USB devices during sudden electrical/mechanical movements.

**Applies to**: S7, S5, and S3 MCU Series

# 7. Known Issues, Limitations, and Additional Usage Notes for SSP v1.7.8

## 7.1 BSP for SSP Supported Platforms

**Issue ID**: 10664

If a user is using the trace buffer for debugging and has data stored in the RAM at addresses above 0x2000 4000, that data will be overwritten by the trace buffer when debugging.

**Applies to**: S128 and S1JA MCU Groups

**Workaround**: The S128 linker script currently allocates 1K for the trace buffer at 0x2000 0000. This allocation could be removed, freeing up the 1K mistakenly reserved for the trace buffer. Using the e$^2$ studio trace buffer function will store 1K of the trace buffer data beginning at 0x2000 4000, so that 1K of RAM must not be used by the application if the trace buffer is to be used for debugging.

**Issue ID**: 15837

Single linker script is available for all S5D5 devices, while these devices have different memory footprints.

**Applies to**: S5 MCU Series

**Workaround**: Update the memory regions in the linker script manually.

## 7.2 Crypto/r_sce

**Issue ID**: 11147

Only data input lengths that are multiples of AES block size are supported for AES encryption/decryption APIs for XTS chaining mode.

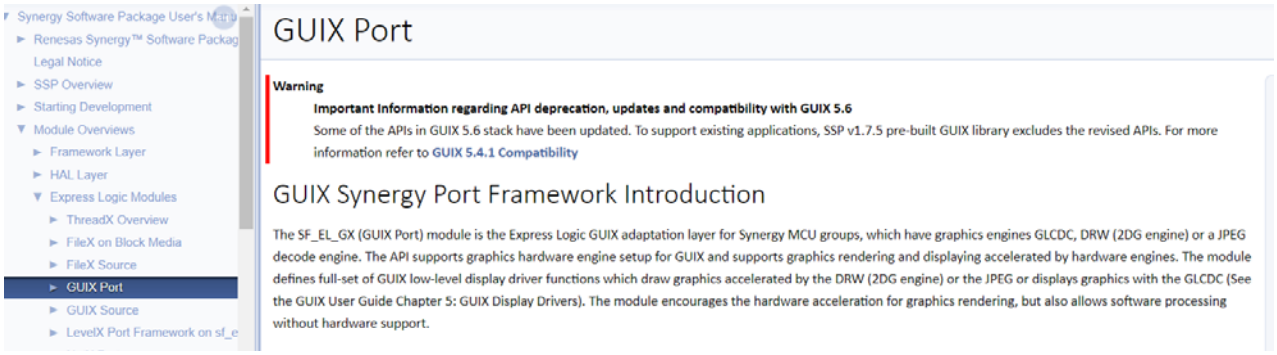
**Applies to**: S7, S5, and S3 MCU Series

**Workaround**: None

## 7.3 GUIX

**Important Information regarding API deprecation, updates, and compatibility with GUIX 5.6**

Some of the APIs in GUIX 5.6 stack have been updated or deprecated and replaced with enhanced versions; additionally, there are changes in the stack that could potentially impact compatibility of existing applications that use GUIX when upgrading to SSP v1.7.8. For more information on these changes and compatibility mode settings for GUIX, refer to the Module Usage Notes for GUIX Port module under the Module Overviews section in the SSP v1.7.8 User's Manual.




**Issue ID**: 16051

An application using fonts with 1 bpp and 4 bpp format along with hardware rendering will give a compilation error.

**Applies to**: S7G2 and S5D9 MCU Groups

**Workaround**: None

## 7.4 ISDE User Experience

**Issue ID**: 7665

When using the Synergy Software Configurator in e² studio/SSC, if you rename a thread on the Threads tab and generate code, a new thread_entry.c file is created with template content, and the old thread_entry.c file remains in the project. If you have edited the thread_entry.c file, your changes are not moved to the new file. The old file remains in the project. It will not be called; it causes a build error if not removed from the project manually.

**Applies to**: All MCUs

**Workaround**: Manually move any edits (if made) from the old thread_entry.c file to the new thread_entry.c file, then manually delete the old thread_entry.c file from your project.

**Issue ID**: 12826

If the Synergy Configuration window is maximized in e² studio, the property window will not be updated.

**Applies to**: All MCUs

**Workaround**: Do not maximize the Synergy Configuration window before clicking on elements when editing the properties.

**Issue ID**: 12908

**Applies to**: All MCUs

A multiple symbol definition error may occur during linkage if an X-Ware library component and the corresponding source component such as ux and ux_src are included. If this occurs, remove the library such as libux.a from the list of libraries used by the linker.

For GCC, this in the **Cross ARM C Linker** > **Libraries section of the C/C++ Build** > **Settings** in the project **Properties**.

For IAR, this in the **IAR Linker for ARM** > **Library section of the C/C++ Build** > **Settings** in the project **Properties**.

Module Names: ux (USBX), tx (ThreadX), nx (NetX), nxd (NetX Duo), fx (FileX), gx (GUIX), ux_host_class_XXX (USBX Host Classes), ux_device_class_XXX (USBX Device Classes).

**Issue ID**: 13854

When debugging a project with a large number of threads (for example, 150 threads) with the RTOS Resource view open, e² studio might hang and become unresponsive.

**Applies to**: All MCUs

**Workaround**: Make the RTOS Resource View small and expand it once the Debug Tree View has finished updating.

## 7.5 NetX

**Issue ID**: 12951

Users will not be able to use TLS 1.0 for secure connection.

**Applies to**: S7G2, S5D9, S5D5, and S5D3 MCU Groups

**Workaround**: None

**Issue ID**: 14293

Build warnings will be observed on compiling NetX Duo BSD application with GCC7 compiler.

**Applies to**: CM4 MCUs (S7, S5, and S3 MCU Series)

**Workaround**: None

## 7.6 nxd_tls_secure

**Issue ID**: 14714

For ECC Cipher Suite with AES GCM Cipher algorithm, the output buffer size is defined as 2048 bytes.

If the incoming message is greater than 2048 bytes, data transfer will fail.

**Applies to**: S7 and S5 MCU Series

**Workaround 1**:

The application should breakdown a large data buffer into 2K chunks.

**Workaround 2**:

- Define NX_CRYPTO_AES_OUTPUT_BUFFE_SIZE to 4096 in `sf_el_nx_crypto\nx_crypto_aes_sce.h`
- Increase the metadata buffer size for the application accordingly.

**Issue ID**: 15051

Warnings will be observed on compiling nxd applications with GCC7.

**Applies to**: S7 and S5 MCU Series

**Workaround**: None

## 7.7 Pin Mapping Issues

**Issue ID**: 10864

The pin configuration tab in the configurator cannot be used to configure the opamp or analog comparators for every use case.

**Applies to**: S7G2, S5D9, S5D5, S5D3, S3A7, S3A3, S128, S124 MCU Groups

**Workaround**: Configure the pins manually in user defined code.

**Issue ID**: 12261

The DAC8 output pin is not being configured when it is configured through ISDE.

**Applies to**: S3A3, S128, and S1JA MCU Groups

**Workaround**: Configure the DAC8 output pin manually.

**Issue ID**: 14452

The current driver uses AVCC0 as the reference voltage for internal ADC. When internal voltage measurement or VREFH0, VREFL0 is selected, pin conflict is observed in the tools and the driver does not support these features.

**Applies to**: S3 and S1 MCU Series

**Workaround**: None

## 7.8 r_agt_input_capture

**Issue ID**: 15070

While capturing the pulse width with AGT input capture, after measurement completion, the counter and overflow value returned from callback are correct, but the same values read simultaneously with lastCaptureGet API are incorrect.

**Applies to**: All MCUs

**Workaround**: None

## 7.9 r_cgc

**Issue ID**: 15945

The SCKDIVCR register bits 18 to 16 are not initialized as expected in cgc initialization because of which the processor is put in a state where it has issues with JLINK connectivity. Note that this issue is observed only with certain clock frequencies.

**Applies to**: S3A6 MCU Group

**Workaround**: Use a different clock frequency.

## 7.10 r_ctsu

**Issue ID**: 6927

`R_CTSU_Update_Parameters()` returns error. Not all return codes are described in the function header.

Some return codes are as follows:

SSP_ERR_NOT_OPEN when mode is set to CTSU_MODE_UNCONFIGURED

SSP_ERR_IN_USE when Measurement Status Counter set to non-zero value or CTSU Data Transfer Status flag is set.

SSP_ERR_CTSU_RC_OVERFLOW when CTSUROVF flag is set

SSP_ERR_CTSU_SC_OVERFLOW when CTSUSOVF flag is set

SSP_ERR_CTSU_ICOMP when TSCAP Voltage Error Monitor flag is set

**Applies to**: All MCUs

**Workaround**: In cases where the returned error code is not described in the function header, refer to the description of the return code in `ssp_common_api.h`.

**Issue ID**: 6928

If the customer calls `R_CTSU_Read` while the driver is in an uninitialized state, then the documented return code is SSP_SUCCESS, but the actual return code is SSP_ERR_NOT_OPEN. When calling `R_CTSU_Read` while the driver is uninitialized, the application should expect a return code of SSP_ERR_NOT_OPEN.

The `R_CTSU_Read()` function is not sufficiently tested with the
CTSU_READ_FILTERED_REF_ICO_VALUES_SEL and
CTSU_READ_FILTERED_REF_ICO_VALUES_ALL options

**Applies to**: All MCUs

**Workaround**: None

**Issue ID**: 6929

Auto-calibration, auto-scan and auto-drift compensation features are not available in the `r_ctsu` driver.

**Applies to**: All MCUs

**Workaround**: None

**Issue ID**: 6931

Parameter checking for NULL parameters is not implemented. Passing in a NULL parameter to the r_ctsu API will result in undefined system operation.

**Applies to**: S7G2, S5D9, S5D5, S3A7, S128, and S124 MCU Groups

**Workaround**: When using this driver, make sure that the control structure passed to `r_ctsu` API is not NULL.

**Issue ID**: 8731

In case of a hardware issue where the channel capacitance has an invalid value (due to board layout), the CTSU data acquisition fails. The code waits in a loop for the data, and does not return.

**Applies to**: All MCUs

**Workaround**: Ensure that the PCB design provides adequate parasitic capacitance per the design layout guidance.

## 7.11 r_riic

**Issue ID**: 16047

When the user opens the `r_iic` module in fast mode and tries to communicate with IIC `read()` or `write()`, there is some SCL clock deviation from its expected value (that is, 400KHz). This is because when the BRCL and BRCH register values are calculated to generate the expected clock (in the `riic_clock_settings()` in the `r_iic open()`), the SCLn line rise time (tr), fall time (tf) and Number of digital noise filters (nf) are not included in the calculation.

**Applies to**: All MCUs

**Workaround**: None

**Issue ID**: 16048

In the function `riic_abort_hw_master()`in the file `r_riic.c`, the RIIC register values are not restored after IIC internal reset. Due to this, whenever a NACK is received on the IIC bus, and the application hits the function `riic_abort_hw_master()`as a part of NACK error handling, it is observed that bit rate after error handling varies when compared to prior to error handling.

**Applies to**: All MCUs

**Workaround**: None

## 7.12 r_sci_spi

**Issue ID**: 10962

Each MCU supports a different range of bit rates depending on the speed of the clock provided to the SCI-SPI peripheral. To get the maximum supported bit rate for a particular MCU, see the corresponding MCU User's Manual.

**Applies to**: All MCUs

**Workaround**: None

**Issue ID**: 15574

In an application, if using DTC for data transfer, SCI SPI can experience an overrun error if the same application makes heavy use of DMAC and/or another DTC instance. This is because the DMAC has a high priority over DTC in arbitration for the mastership of the DMA bus. Also, arbitration between different triggers/transfers in DTC is done based on the interrupt/trigger priority. So, if the DMAC or DTC triggered by high priority interrupt/task is accessing the DMA bus and SCI SPI is receiving the data at the same time, DTC used by SCI SPI will not be able to access the bus to transfer the received data into the memory, causing SCI SPI to return an overrun error.

**Applies to**: All MCUs

**Workaround**: Overrun error can be averted with one of the following options:

1. If SCI SPI uses DTC for data transfer, avoid the use of DMAC or another DTC instance in an application.
2. If DMAC/DTC is a must for other data transfers, avoid the use of DTC with SCI SPI.
3. Use RSPI instead of SCI SPI. The RSPI hardware can handle overrun conditions.

## 7.13 r_sci_uart

**Issue ID**: 16028

When `baudSet()` API is used to set the baud rate, the user receives one byte less, and the first two bytes of the actual send data are swapped.

**Applies to**: S3 and S1 MCU Series

**Workaround**:

1. Re-enable the TE bit in the `baudSet()` function.
2. Set baud rate in stack properties.

## 7.14 r_sdmmc

**Issue ID**: 15942

When doing a write operation with FileX with r_sdmmc as the underlying layer, and with r_sdmmc property WP(write protect) set to "Not Used", and the corresponding WP pin in pin configuration set to "NONE"(as it is unused), the write operation fails.

**Applies to**:S5D9 and S5D3 MCU Groups

**Workaround**: The write passes when the WP pin in pin configuration is set to its hardware pin instead of to "NONE."

## 7.15 sf_ble

**Issue ID**: 9225

HID profile client mode is not supported by RL78G1D. As a result, the BLE framework implementation of the HID profile will also not support the HID profile client mode. Applications using a BLE framework for RL78G1D will not be able to use the HID profile in client mode.

**Applies to**: All MCUs

**Workaround**: None

**Issue ID**: 9256

The projects using RL78G1D framework will see compilation warnings. All the warnings are in the 3rd party RL78G1D driver code and will not have impact on the user applications. The RL78G1D framework files do not have any warnings.

**Applies to**: RL78G1D on all Synergy MCUs

**Workaround**: None

## 7.16 sf_cellular

**Issue ID**: 14566

Automatic time zone update disable functionality does not work. Even when the user disables automatic time zone update, the current updated time is received.

**Applies to**: CAT3, CAT1, and Quectel BG96 modules

**Workaround**: None

## 7.17 sf_el_gx

**Issue ID**: 15783

Build warnings are being observed when compiling GUIX Source with GCC 7.2.1.

**Applies to**: S7G2 and S5D9 MCU Group

**Workaround**: None

## 7.18 sf_el_tx

**Issue ID**: 13678

SF_CONTEXT_SAVE and SF_CONTEXT_RESTORE (in `bsp_common.h`) should only be defined if TX_ENABLE_EXECUTION_CHANGE_NOTIFY or TX_ENABLE_EVENT_TRACE is defined.

**Applies to**: All MCUs

**Workaround**: None

## 7.19 sf_el_ux

**Issue ID**: 8574

The current sf_el_ux HCD driver does not enable the double buffer feature for bulk out PIPEs, which is supported by USB hardware. Because of that, USB data throughput for data write through a bulk out PIPE will be less than the value for double buffer-enabled. This issue is only for data write (bulk OUT). Double buffering is supported for data read (bulk IN).

**Applies to**: S7, S5, and S3 MCU Series

**Workaround**: None

**Issue ID**: 11332

SF_EL_UX DCD driver is not functional when configuring DTC as a transfer component to the USBX Class stack in the Synergy Configuration tool.

In the USBX DCD Port driver (sf_el_ux Device Controller Driver), when DTC is selected as the transfer component in the stack configuration series, the compilation errors that were displayed earlier for the S1 MCU Series are no longer displayed (for S124, S128, S1JA MCU Groups).

On non-S1 MCUs (that is S7, S5, and S3 MCU Series), there are no compilation errors (build is success) but the DCD driver is not functional.

**Applies to**: All MCUs

**Workaround**: None

**Issue ID**: 13481

The USB host sends out a PING packet after receiving NAK or NYET handshake from the device. However, it also sends out a PING packet for ACK handshake, which is not expected behavior according to the USB 2.0 specification.

**Applies to**: All Synergy MCUs supporting USBX Host

**Workaround**: None

**Issue ID**: 13528

In the USBX Device Class CDC, in blocking mode, write/read calls made to the sf_el_ux DCD driver do not support the timeout feature, which may result in indefinite waiting for the host transfer to get completed.

Option 1: In order to use the non-blocking or callback mode in USBX CDC device class, call the `ux_device_class_cdc_acm_ioctl()` API in the application to use transmission with callback. See the latest *USBX Device Stack User Guide* for more information on the Device Class APIs.

Option 2: Call the `ux_device_stack_transfer_abort()` API from the other threads in the application to abort the pending transfer requests.

**Applies to**: All MCUs

**Workaround**: None

**Issue ID**: 15368

`ux_host_class_printer_name_get` function does not support all IEEE 1284 Device ID strings.

**Applies to**: S7G2 and S5D9 MCU Group

**Workaround**: None

**Issue ID**: 15873

In USBX Device CDC class, `write` API `_ux_device_class_cdc_acm_write()` is used to send data to CDC host. But, `write` API returns completion status earlier than the actual write operation completes.

**Applies to**: All MCUs

**Workaround**: None

## 7.20 sf_i2c

**Issue ID**: 14618

With GCC 7.2 and optimization level -Og, sf_i2c `read` API (with sci_i2c driver) intermittently hangs when invoked with a timeout value of 0 instead of returning timeout error.

**Applies to**: All MCUs

**Workaround**:

- Use optimization level -O2.
- Instead of sci_i2c, use r_riic as the lower-level driver.

## 7.21 sf_touch_ctsu

**Issue ID**: 6858

1. When a channel is set to NULL, `SF_TOUCH_CTSU_Read()` returns SSP_ERR_INTERNAL.
2. Return values from ThreadX API calls are not checked in the framework. This can lead to functional issues in the framework when ThreadX APIs return error. Framework may not work as expected in such error cases since errors are not handled.
3. With valid callback and context if callback_index is set to SF_TOUCH_CTSU_CFG_MAX_WIDGET_TYPES ( = 3 ), `SF_TOUCH_CTSU_Open()` returns SSP_ERR_OUT_OF_MEMORY.

**Applies to**: All MCUs

**Workaround**: None

**Issue ID**: 6859

`SF_TOUCH_CTSU_Read()` returns error value SSP_ERR_INTERNAL if semaphore get or put are not successful.

**Applies to**: All MCUs

**Workaround**: None

## 7.22 sf_touch_ctsu_button

**Issue ID**: 6882

1. valid range for `button_count` is 0 to less than SF_TOUCH_CTSU_BUTTON_CFG_USER_SUPPORTED_BUTTONS ( = 12)
2. For `button_count` values outside the range, SF_TOUCH_CTSU_Button_Open() returns error SSP_ERR_ASSERTION .

**Applies to**: All MCUs

**Workaround**: None

**Issue ID**: 6883

For `button_count` values outside the range, `SF_TOUCH_CTSU_Button_Open()` returns error SSP_ERR_ASSERTION and hence buttons outside the range cannot be operated.

**Applies to**: All MCUs

**Workaround**: Button_count values must be set to value 0 to less than SF_TOUCH_CTSU_BUTTON_CFG_USER_SUPPORTED_BUTTONS ( = 12).

## 7.23 sf_Wifi

**Issue ID**: 8394

The projects using GT202 framework will see compilation warnings. All the warnings are in the 3rd party GT202 driver code. The GT202 framework files do not have any warnings. The warnings should not impact the user applications.

**Applies to**: WiFi Framework for GT202 on S7G2, S3A7, S5D9, S5D5, S3A6 (only socket), S3A3 MCU Groups

**Workaround**: None

**Issue ID**: 12742

GT202 module supported by WiFi Framework is affected by WPA2 KRACK issue.

**Applies to**: GT202 module supported by WiFi Framework

**Workaround**: None

**Issue ID**: 14126

WiFi WPS functionality does not work with WPA security.

**Applies to**: WiFi Framework using GT202

**Workaround**: None

**Issue ID**: 14314

If an ongoing WPS session gets terminated by a peer WiFi device, then the GT202 driver hangs. The GT202 driver API for WPS is called by invoking WiFi Framework APIs which use mutex. When GT202 driver hangs, it will cause the WiFi WPS API to hang, resulting in WiFi APIs returning mutex error.

**Applies to**: All MCUs supported by GT202

**Workaround**: None

**Issue ID**: 15793

1. In `netx_next_received_packet` (() function , **else** part of the condition (`(length - *p_total_len) < data_len`) is not reachable.

   This piece of code performs packet fragmentation and the GT202 does not perform packet fragmentation and hence the piece of code is not executed.
2. In function `gt202_wps_start()`, **else** part of condition `if (SSP_SUCCESS == ssp_err)` is not reachable. That is, table for mapping GT202 error to SSP error (`sf_wifi_gt202_ssperr_map`) always returns SSP_SUCCESS (as Net parameter `net_params` is initialized with 0 and holds same value throughout) irrespective of inputs, this causes unreachable branch.

The value of `net_params` may be altered by the call:

```
ioctrl_struct.data = ((QOSAL_VOID *) &net_params);

ioctrl_struct.length = sizeof(net_params);

retval = ath_ioctl_handler (&p_driver_handle->enet, &ioctrl_struct);
```

In which case the `if(SSP_SUCCESS == ssp_err)` may not always be equal to SSP_SUCCESS.

**Applies to**: All MCUs

**Workaround**: None

## 7.24 SSP IAR Support

**Issue ID**: 12845

Cannot debug the program when selecting the option **Download and Debug** in EWSYN or **Debug** in e$^2$ studio for the first time after setting an ID code in the project.

**Applies to**: All MCUs

**Workaround**: When the debug fails, select the option to **Debug without download** in EWSYN or **Debug** in e$^2$ studio again to successfully debug the program.

**Issue ID**: 13900

In some cases, the build fails with the error “Secure builder required” after migrating to a newer SSP version in EWSYN.

**Applies to**: All MCUs

**Workaround**: Select **Project** > **Make (F7)** after the issue occurs. The project should then build without errors.

**Issue ID**: 14485

Library projects which use many/long `include` paths cause the compiler command line to exceed system limit and fails to build the library.

**Applies to**: Projects created with IAR compiler in e$^2$ studio.

**Workaround**: None

## 7.25 SSP XMLs for ISDEs

**Issue ID**: 12857

Creating a project with a custom board pack might not reflect the customized values set for the properties in that custom board pack.

**Applies to**: All MCUs

**Workaround**: None

## 7.26 Synergy Tools

**Issue ID**: 11556

Synergy builder is excluded from the tool command pattern when changing the toolchain from IAR 7.x to IAR 8.x, which leads to a build error that the secure builder is required when trying to build the project after migrating.

**Applies to**: All MCUs

**Workaround**:

The following workaround can be used to migrate projects with IAR 7.x to IAR 8.x:

1. Add environment variable `SECURE_BUILD_COMMAND`: `${renesas.support.targetLoc:synergy-build} /isdebuild`
2. Update command line pattern IAR C/C++ Compiler for ARM setting if the following command is missing: `${SECURE_BUILD_COMMAND}`
3. Update command line pattern IAR C/C++ Assembler for ARM if the following command is missing: `${SECURE_BUILD_COMMAND}`

**Issue ID**: 12584

An error occurs when setting the watchpoint at certain addresses. Debug sessions cannot be started when these watchpoints with errors are still present.

**Applies to**: S5D9 MCU Group

**Workaround**: Remove the watchpoints from the breakpoints view and start the debug session.

**Issue ID**: 12925

When exporting the project, selecting the option for `.tar` format does not export the project in `.tar` format, but exports it in `.zip` format.

**Applies to**: Tools

**Workaround**: Edit the archive file name field by replacing the `.zip` with `.tar`, and the project will be exported in `.tar` format.

**Issue ID**: 14436

Some of the old projects with customized stacks might fail after migrating to e$^2$ studio v7.3 because the default modules get repopulated in the stack.

**Applies to**: All MCUs

**Workaround**: The user explicitly needs to delete the modules that are repopulated after migration.

**Issue ID**: 14747

When SSP v1.6.0 and a version later than SSP v1.6.0 are both installed, Developer assistance node in the project created with SSP v1.6.0 shows the function `wpsstart,` which is not supported in SSP v1.6.0. Dragging and dropping the API to the source file will a show message about an unresolved method.

**Applies to**: Projects created with SSP v1.6.0 and using the RDS file created with later versions of SSP

**Workaround**: Do not drag and drop the `wpsstart` function from the Developer Assistant node in SSP v1.6.0.

**Issue ID**: 15093

Using the option "Rename and import existing C/C++ project" causes intermittent failure in importing the project, and gives an error message.

**Applies to**: All MCUs

**Workaround**: None

**Issue ID**: 15104

e$^2$ studio v7.3.0 is sensitive with respect to the casing of linker script file names. This is experienced only in the projects created with the previous version of e$^2$ studio where the linker script names do not exactly match in casing. In this case, the customer would experience a build error saying that the linker script is not found.

**Applies to**: All MCUs

**Workaround**: If the build is failing with **.ld not found** error, go to the linker configuration in e$^2$ studio project properties and delete the linker script entry.

**Issue ID**: 15203

When performing a clean build of a project in command line, the debug build configuration fails to be cleaned as the length of the `rm` command line has not adhered to the limit of the console interface.

**Applies to**: All MCUs

**Workaround**: None

**Issue ID**: 15330

Projects created with SSP versions prior to SSP v1.6.3 and edited to remove the default lower module fail to build when migrated to SSP v1.6.3.

**Applies to**: Projects created in earlier versions that have been edited by removing the default lower level module in thread stacks

**Workaround**: Open the threads tab before building the project

**Issue ID**: 15339

Default property value of the IP address does not get picked up for existing projects after changes to the pack. Opening existing projects shows the previously saved value instead of the default value from the pack.

**Applies to**: Projects which use the packs with the change for IP address

**Workaround**: None

**Issue ID**: 15536

In e$^2$ studio 7.4, only threads that have a run count greater than 0 will be shown in the **Debug** view. When one of the threads has a run count of 0, all the threads after that check do not populate in the **Debug** view.

**Applies to**: All MCUs

**Workaround**: None

**Issue ID**: 15606

When starting to debug a project, sometimes the program stops executing after clicking resume at the reset_handler.

**Applies to**: All MCUs

**Workaround**: Click reset or restart button to continue running the program

**Issue ID**: 15653

The Synergy project fails to compile when including the macros `_has_include` or `_has_include_next`.

**Applies to**: All MCUs

**Workaround**: Go to the properties of the source file where the macro has been added and remove the `${SECURE_BUILD_COMMAND}` from the command line pattern. The project should now compile properly.

**Issue ID**: 15685

Stack Analysis view cannot install when selecting a Synergy device in the installer.

**Applies to**: All MCUs

**Workaround**: One of the following workarounds can be used to fix the issue:

1. Add the Stack Analysis plugin by re-launching installer with "Modify" option
2. Add the plugin through **Help** > **Install New Software**.

## 7.27 Tes

**Issue ID**: 14095

The rendering of concave polygons is not supported when D/AVE 2D drawing engine is enabled.

**Applies to**: S7G2 and S5D9 MCU Groups

**Workaround**: Disable D/AVE 2D drawing engine to render concave polygons.

**Issue ID**: 15762

An application using pixelmaps to fill the shapes does not render pixelmaps properly inside the shapes if the pixelmaps width and height are not the power of 2.

**Applies to**: S7G2 and S5D9 MCU Groups

**Workaround**: The pixelmaps are properly drawn inside the shapes if pixelmap width and height are the power of 2.

## 7.28 Tools Development

**Issue ID**: 15202

TraceX fails to launch and gives a license error when an existing TraceX installation is overwritten by reinstalling TraceX using TraceX standalone installer.

**Applies to**: All MCUs

**Workaround**: Uninstall the existing TraceX application and install it again.

## 7.29 USBX

**Issue ID**: 8647

The USB throughput for file `read/write` operation with USBX Device Class Mass Storage is not consistent and may vary for every measurement.

**Applies to**: All MCUs

**Workaround**: None

**Issue ID**: 14100

Warnings for “this statement may fall through” will be observed when compiling USBX Device class source code.

**Applies to**: All MCUs

**Workaround**: None

**Issue ID:** 15857

An infinite loop occurs when a large file is copied on an SD card by using USBFS (DMA enable) with the IAR compiler.

**Applies to**: All MCUs

**Workaround:** USBFS (CPU) with the IAR compiler or USBFS (DMA enable) with the GCC compiler can be used.

**Issue ID**: 15990

The Mode Sense function `_ux_device_class_storage_mode_sense` sets the WP information in the wrong mode parameter header format. USBX device mass storage class application will not be able to notify the host regarding the write protection information of the storage media.

Applies to: All MCUs

**Workaround**: None

**Issue ID**: 16007

USB CDC ACM fails to receive data only when 64 bytes are sent. But when multiples of 64 bytes are transferred, USB CDC ACM receives data properly.

**Applies to**: All MCUs

**Workaround**: None

# 8. Complete List of Modules Supported in this Release

These modules are available on the respective MCUs based on the following criteria:

- If the core functionality of the module has been tested and works on an MCU, even if it has known bugs, then the module is supported on the MCU.
- If the core functionality is broken or not tested on an MCU, then that module is not supported on the MCU.
- If a module is independent of the underlying MCU hardware or HAL drivers, and has been tested on a particular Synergy MCU, the following table indicates that this module is supported on all the Synergy MCUs that the underlying driver/framework/stack depend on have been tested.

## 8.1 BSP and Driver Modules Available in this Release

| Module Name | SSP Feature | Supported Synergy MCU Groups |
|---|---|---|
| BSP | Board Support Package | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_acmphs | Analog Comparator High Speed | S1JA, S3A7, S5D9, S5D5, S5D3, S7G2 |
| r_acmplp | Analog Comparator Low Power | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7 |
| r_adc | A/D Converter | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_agt | Asynchronous General Purpose Timer | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_agt_input_capture | AGT Input Capture | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_analog_connect | Analog Connect | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_cac | Clock Frequency Accuracy Measurement Circuit | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_can | Controller Area Network | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_cgc | Clock Generation Circuit | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_crc | Cyclic Redundancy Check Calculator | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_ctsu | Capacitive Touch Sensing Unit | S124, S128, S3A7, S5D5, S5D9, S7G2 |
| r_dac | Digital to Analog Converter | S124, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_dac8 | 8-bit Digital to Analog Converter | S128, S1JA, S3A1, S3A3, S3A6 |
| r_dmac | Direct Memory Access Controller | S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_doc | Data Operation Circuit | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_dtc | Data Transfer Controller | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_elc | Event Link Controller | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_flash_hp | Flash Memory, High Performance | S5D3, S5D5, S5D9, S7G2 |
| r_flash_lp | Flash Memory, Low Power | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7 |
| r_fmi | Factory Microcontroller Information | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_glcd | Graphics LCD Controller | S5D9, S7G2 |
| r_gpt | General Purpose Timer | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |

| Module Name | SSP Feature | Supported Synergy MCU Groups |
|---|---|---|
| r_gpt_input_capture | General Input Capture | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_icu | Interrupt Controller Unit | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_ioport | General Purpose I/O Ports | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_iwdt | Independent Watchdog Timer | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_jpeg_common | JPEG Common | S5D9, S7G2 |
| r_jpeg_decode | JPEG Decode | S5D9, S7G2 |
| r_jpeg_encode | JPEG Encode | S5D9, S7G2 |
| r_kint | Keyboard Interrupt Interface | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_lpm† | Low Power Mode | S124, S3A7, S7G2 |
| r_lpmv2_s1ja | Low Power Mode V2 for S1JA | S1JA |
| r_lpmv2_s124 | Low Power Mode V2 for S124 | S124 |
| r_lpmv2_s128 | Low Power Mode V2 for S128 | S128 |
| r_lpmv2_s3a1 | Low Power Mode V2 for S3A1 | S3A1 |
| r_lpmv2_s3a3 | Low Power Mode V2 for S3A3 | S3A3 |
| r_lpmv2_s3a6 | Low Power Mode V2 for S3A6 | S3A6 |
| r_lpmv2_s3a7 | Low Power Mode V2 for S3A7 | S3A7 |
| r_lpmv2_s5d3 | Low Power Mode V2 for S5D3 | S5D3 |
| r_lpmv2_s5d5 | Low Power Mode V2 for S5D5 | S5D5 |
| r_lpmv2_s5d9 | Low Power Mode V2 for S5D9 | S5D9 |
| r_lpmv2_s7g2 | Low Power Mode V2 for S7G2 | S7G2 |
| r_lvd | Low Voltage Detection Driver | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_opamp | Operational Amplifier | S128, S1JA, S3A1, S3A3, S3A6, S3A7 |
| r_pdc | Parallel Data Capture Unit | S5D5, S7G2 |
| r_qspi | Quad Serial Peripheral Interface | S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_riic | IIC | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_riic_slave | IIC Slave | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_rspi | Serial Peripheral Interface | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_rtc | Real-time Clock | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_sci_i2c | Serial Communication Interface I2C | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_sci_spi | Serial Communication Interface SPI | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_sci_uart | Serial Communication Interface UART | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_sdadc | Sigma Delta ADC | S1JA |
| r_sdmmc | SDHI Driver for SDIO and SD/MMC Memory Devices | S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_slcdc | Segment LCD Controller | S3A1, S3A3, S3A6, S3A7 |
| r_ssi | (Inter-IC Sound) Interface [old: Serial Sound Interface] or r_i2s | S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |

| Module Name | SSP Feature | Supported Synergy MCU Groups |
|---|---|---|
| r_wdt | Watchdog Timer | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| r_sce[#] | Cryptographic Library (HAL interfaces) | See table note on Cryptographic Functions |

[#] **Cryptographic Functions**: Section 8.4 lists cryptographic functions available for each MCU in this release; these functions are accessible as part of r_sce/cryptographic library.

## 8.2 Framework Modules Supported in this Release

| Module Name | SSP Feature | Supported Synergy MCU Groups |
|---|---|---|
| sf_adc_periodic | Periodic Sampling ADC | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_audio_playback | Audio Playback | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_audio_playback_hw_dac | Audio Playback HW DAC | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_audio_playback_hw_i2s | Audio Playback HW I2S | S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_audio_record_adc | Audio Record ADC | S124, S128, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_audio_record_i2s | Audio Record I2S | S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_ble_rl78g1d | BLE Framework | S124, S128, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_ble_rl78g1d_onboard_profile | BLE Framework Onboard Profiles | S124, S128, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_block_media_lx_nor | Block Media Interface for LevelX NOR | S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_block_media_qspi | Block Media Interface for QSPI | S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_block_media_ram | Block Media Interface for RAM | S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_block_media_sdmmc | Block Media Interface for SD Multi Media Card | S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_comms_telnet | Telnet Communications | S5D3, S5D5, S5D9, S7G2 |
| sf_console | Console | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_el_fx | Synergy FileX interface | S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_el_gx | Synergy GUIX Interface | S5D9, S7G2 |
| sf_el_lx_nor | Synergy LevelX NOR Interface | S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_el_nx | Synergy NetX Interface | S5D5, S5D9, S7G2 |
| sf_el_nx_comms | Synergy NetX Communication Interface | S5D5, S5D9, S7G2 |
| sf_el_ux | Synergy USBX Interface | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_el_ux_comms† | Synergy USBX Communication Interface | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_el_ux_comms_v2 | Synergy USBX Communication Interface V2 | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |

| Module Name | SSP Feature | Supported Synergy MCU Groups |
|---|---|---|
| sf_external_irq | External Interrupt | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_i2c | I2C Framework | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_jpeg_decode | JPEG Decode | S5D9, S7G2 |
| sf_memory_qspi_nor | Memory QSPI NOR | S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_message | Inter-Thread Messaging | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_power_profiles† | Power Mode Profile | S124, S3A7, S7G2 |
| sf_power_profiles_v2 | Power Mode Profile V2 | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_spi | SPI Framework | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_tes_2d_drw | 2D Drawing Engine Framework | S5D9, S7G2 |
| sf_thread_monitor | Thread Monitor (Watchdog) | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_touch_ctsu | Capacitive Touch Sensing Unit | S124, S128, S3A7, S5D9, S7G2 |
| sf_touch_ctsu_button | Capacitive Touch Sensing Unit Button | S124, S128, S3A7, S5D9, S7G2 |
| sf_touch_ctsu_slider | Capacitive Touch Sensing Unit Slider | S124, S128, S3A7, S5D9, S7G2 |
| sf_touch_panel_i2c | Touch Panel I²C | S5D9, S7G2 |
| sf_touch_panel_v2 | Touch Panel Version 2 | S5D9, S7G2 |
| sf_uart_comms | UART Framework | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_wifi_gt202 | WiFi Framework | S124, S128, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_wifi_gt202_onchip | WiFi framework on Chip Stack | S124, S128, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_cellular_catm1 | Cellular Framework Quectel BG96 CATM1 | S5D9, S7G2 |
| sf_cellular_catm1_socket | Cellular Framework Quectel BG96 CATM1 Socket | S5D9, S7G2 |
| sf_cellular_cat1 | Cellular Framework Nimbelink CAT1 | S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_cellular_cat1_socket | Cellular Framework Nimbelink CAT1 Socket | S128, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_cellular_cat3 | Cellular Framework Nimbelink CAT3 | S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_cellular_cat3_socket | Cellular Framework Nimbelink CAT3 Socket | S128, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_crypto#, ## | Cryptographic Framework | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| sf_el_nx_crypto | Cryptographic Framework-Shim layer | S5D3, S5D5, S5D9, S7G2 |

# **Cryptographic Functions**: Section 8.4 lists cryptographic functions available for each MCU in this release; these functions are accessible as part of r_sce/cryptographic library.

## Framework Interfaces for Cryptographic Functions (sf_crypto) available for this release include: HASH, TRNG, and Key Generation (RSA and AES), Key Installation, Signature, and Cipher.

† Indicates a module that is deprecated starting with SSP v1.3.0 and all subsequent versions. Deprecated modules will only be available to maintain compatibility with existing projects that may be using them. It is highly recommended that new projects use the recommended replacements and not use deprecated modules. For details, see the *SSP User's Manual*.

## 8.3 Third-Party Modules Supported in this Release

| Module Name | SSP Feature | Supported Synergy MCU Groups |
|---|---|---|
| fx | FileX | S124, S3A3, S3A6, S3A7, S5D9, S7G2 |
| gx | GUIX | S5D9, S7G2 |
| nx | NetX | S5D9, S7G2 |
| nx_auto_ip | NetX Auto IP | S5D9*, S7G2 |
| nx_bsd | NetX BSD | S5D9*, S7G2 |
| nx_dhcp_client | NetX DHCP Client | S5D9*, S7G2 |
| nx_dhcp_server | NetX DHCP Server | S5D9*, |
| nx_dns_client | NetX DNS Client | S5D9*, S7G2 |
| nx_ftp_client | NetX FTP Client | S5D9*, S7G2 |
| nx_ftp_server | NetX FTP Server | S5D9*, S7G2 |
| nx_http_client | NetX HTTP Client | S5D9*, S7G2 |
| nx_http_server | NetX HTTP Server | S5D9*, S7G2 |
| nx_pop3 | NetX POP3 | S5D9*, S7G2 |
| nx_ppp | NetX PPP | S5D9*, S7G2* |
| nx_smtp_client | NetX SMTP Client | S5D9*, S7G2 |
| nx_snmp | NetX SNMP | S5D3*, S5D5*, S5D9*, S7G2 |
| nx_sntp_client | NetX SNTP Client | S5D9*, S7G2 |
| nx_telnet_client | NetX Telnet Client | S5D9*, S7G2 |
| nx_telnet_server | NetX Telnet Server | S5D9*, S7G2 |
| nx_tftp_client | NetX TFTP Client | S5D9*, S7G2 |
| nx_tftp_server | NetX TFTP Server | S5D9*, S7G2 |
| nxd | NetX Duo Stack | S5D9, S7G2 |
| nxd_auto_ip | NetX Duo Auto IP | S5D9*, S7G2 |
| nxd_bsd | NetX Duo BSD | S5D9*, S7G2 |
| nxd_dhcp | NetX Duo DHCP IPv4 Client | S5D9*, S7G2 |
| nxd_dhcp | NetX Duo DHCP IPv6 Client | S5D9*, S7G2 |
| nxd_dhcp_server | NetX Duo DHCP IPv4 Server | S5D9*, S7G2 |
| nxd_dhcp_server | NetX Duo DHCP IPv6 Server | S5D9*, S7G2 |
| nxd_dns | NetX Duo DNS Client | S5D9*, S7G2 |
| nxd_ftp_client | NetX Duo FTP Client | S5D9*, S7G2 |
| nxd_ftp_server | NetX Duo FTP Server | S5D9*, S7G2 |
| nxd_http_client | NetX Duo HTTP Client | S5D9*, S7G2 |
| nxd_http_server | NetX Duo HTTP Server | S5D9*, S7G2 |
| nxd_nat | NetX Duo NAT | S5D9*, S7G2 |
| nxd_pop3 | NetX Duo POP3 | S5D9*, S7G2 |
| nxd_ppp | NetX Duo PPP | S5D9*, S7G2* |
| nxd_smtp_client | NetX Duo SMTP Client | S5D9*, S7G2 |
| nxd_snmp | NetX Duo SNMP | S5D3*, S5D5*, S5D9*, S7G2 |
| nxd_sntp_client | NetX Duo SNTP Client | S5D9*, S7G2 |
| nxd_telnet_client | NetX Duo Telnet Client | S5D9*, S7G2 |
| nxd_telnet_server | NetX Duo Telnet Server | S5D9*, S7G2 |
| nxd_tftp_client | NetX Duo TFTP Client | S5D9*, S7G2 |
| nxd_tftp_server | NetX Duo TFTP Server | S5D9*, S7G2 |

| Module Name | SSP Feature | Supported Synergy MCU Groups |
|---|---|---|
| nxd_mqtt_client | NetX Duo MQTT Client | S5D3, S5D5, S5D9, S7G2 |
| nxd_tls_secure | NetX Duo TLS Secure | S5D3, S5D5, S5D9, S7G2 |
| nxd_web_http_client | NetX Duo Web HTTP1.1 Client | S5D5*, S5D9, S7G2 |
| | NetX Duo Web HTTPS Client | S5D5, S5D9, S7G2 |
| nxd_web_http_server | NetX Duo Web HTTP1.1 Server | S5D9, S7G2 |
| | NetX Duo Web HTTPS Server | S5D9, S7G2 |
| Tx | ThreadX | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| Lx_nor | LevelX NOR | S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2 |
| ux_device_class_storage | USBX Device Class Mass Storage | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| ux_device_class_hid | USBX Device Class HID | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| ux_device_class_cdc_acm | USBX Device Class CDC-ACM | S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2 |
| ux_host_class_cdc_acm | USBX Host Class CDC-ACM | S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2 |
| ux_host_class_hid | USBX Host Class HID | S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2 |
| ux_host_class_hub | USBX Host HUB | S5D3, S5D5, S5D9, S7G2 |
| ux_host_class_printer | USBX Host Class Printer | S3A3, S3A7, S5D9, S7G2 |
| ux_host_class_storage | USBX Host Class Mass Storage | S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2 |
| ux_host_class_video | USBX Host Video class | S5D9, S7G2 |

* NetX and NetX Duo Applications are MCU-independent application layer protocols dependent on the NetX and Ethernet drivers. All MCUs on which NetX has been tested and verified support these protocols.

## 8.4 Cryptographic Functions for Each MCU Supported in this Release

| Function | S5D3, S5D5, S5D9, S7G2 | S3A1, S3A3, S3A6, S3A7 | S124, S128, S1JA |
|---|---|---|---|
| TRNG | Generate and read random number | Generate and read random number | Generate and read random number |
| AES | Encryption, decryption, Key Generation - wrapped keys | Encryption, decryption, Key Generation - wrapped keys | Encryption, decryption |
| AES Key Size | 128-bit, 192-bit, 256-bit | 128-bit, 256-bit | 128-bit, 256-bit |
| AES Key Type | Plain text / raw key, wrapped key | Plain text / raw key, wrapped key | Plain text / raw key |
| AES Chaining Modes | ECB, CBC, CTR, GCM, XTS†† | ECB, CBC, CTR, GCM, XTS | ECB, CBC, CTR |
| ARC4 | Encryption, decryption | NA | NA |
| TDES | Encryption, decryption | NA | NA |
| TDES Key Size | 192-bit | NA | NA |
| TDES Chaining Modes | ECB, CBC, CTR | NA | NA |
| RSA | Signature Generation, Signature Verification, Public-key Encryption, Private-key Decryption, | NA | NA |

| Function | S5D3, S5D5, S5D9, S7G2 | S3A1, S3A3, S3A6, S3A7 | S124, S128, S1JA |
|---|---|---|---|
| | Key Generation - plain text and wrapped keys | | |
| RSA Key Size | 1024-bit, 2048-bit | NA | NA |
| RSA Key Type | Plain text / raw key, Wrapped key | NA | NA |
| Key Installation | AES, ECC, RSA keys | AES keys | NA |
| ECC | Key Generation – plain text and wrapped keys, Scalar Multiplication, ECDSA – Signature Generation, ECDSA – Signature Verification | NA | NA |
| ECC Key Size (in bits) | 192-bit, 224-bit, 256-bit, and 384-bit | NA | NA |
| ECC Key Type | Plain text / raw keys and wrapped keys | NA | NA |
| DSA | Signature Generation, Signature Verification | NA | NA |
| DSA Key Size | (1024, 160)-bit, (2048, 224)-bit, (2048, 256)-bit | NA | NA |
| HASH | SHA1, SHA224, SHA256, MD5 | NA | NA |

†† XTS is supported for 128-bit and 256-bit keys only.

## 8.5 Experimental Modules Supported in this Release

Modules that have not been tested on the MCUs have been classified as experimental modules and are listed in the following table. These experimental modules are currently not supported by Synergy Configuration tools and use of these modules in customer projects is not supported by Renesas at this time.

| **Experimental Modules** | | |
|---|---|---|
| **Module Name** | **SSP Feature** | **Supported Synergy MCU Groups** |
| ux_device_class_cdc_ecm | USBX Device Class CDC-ECM | S124, S3A3, S3A7, S5D9, S7G2 |
| ux_device_class_rndis | USBX Device Class RNDIS | S124, S3A3, S3A7, S5D9, S7G2 |
| ux_host_class_gser | USBX Host Class Generic Serial | S3A3, S3A7, S5D9, S7G2 |
| ux_host_class_prolific | USBX Host Class Prolific | S3A3, S3A7, S5D9, S7G2 |
| ux_host_class_swar | USBX Host Class Swar | S3A3, S3A7, S5D9, S7G2 |
| ux_network_driver | USBX Network Driver | S124, S3A3, S3A7, S5D9, S7G2 |

# 9. Additional Technical Notes

- Subscribe to the Synergy Technical Bulletin Board to receive the latest technical news and notifications about new features, known issues, workarounds, and release announcements. To subscribe, visit www.renesasrulz.com/synergy/synergy_tech_notes/f/214.aspx. Sign in to Renesas Rulz, and press **Email Subscribe to this forum**.
- Additional technical information, including informative papers and articles on SSP and Synergy can be found at Synergy Knowledge Base, www.renesas.com/synergy/knowledgebase.

## Website and Support

Visit the following vanity URLs to learn about key elements of the Synergy Platform, download components and related documentation, and get support.

| | |
|---|---|
| Synergy Software | www.renesas.com/synergy/software |
| Synergy Software Package | www.renesas.com/synergy/ssp |
| Software add-ons | www.renesas.com/synergy/addons |
| Software glossary | www.renesas.com/synergy/softwareglossary |
| Development tools | www.renesas.com/synergy/tools |
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## Revision History

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | May 29.20 | - | First release |
| 1.01 | Jun.16.20 | - | Second release |

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