

# SSP v1.5.0

Release Note

Renesas Synergy™ Platform  
Synergy Software  
Synergy Software Package

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## 1. Introduction

This document describes the release notes for **Synergy Software Package (SSP) version 1.5.0**.

## 2. Release information

SSP Release Version	v1.5.0
Release Date	Sep 14, 2018

The intended audience for this release is Renesas Synergy customers, prospective customers, partners, and support staff. This release note describes the new features, enhancements, bug fixes and known issues in SSP v1.5.0 that were identified since the last patch release SSP v1.4.1.

### Notes:

- Users are required to generate and download a new Development and Production License Key file from Synergy Software Package (SSP) page in Renesas Synergy Platform section, on [Renesas.com](http://Renesas.com) and apply it to your projects when upgrading to SSP v1.5.0. Using an older Development and Production License Key file generated/issued prior to SSP v1.5.0 will result in a build failure for the new module, NetX Web.
- To generate and download a new License Key file, log on [Renesas.com](http://Renesas.com) using your existing [MyRenesas](#) or Synergy Gallery credentials, or by creating a new MyRenesas account.

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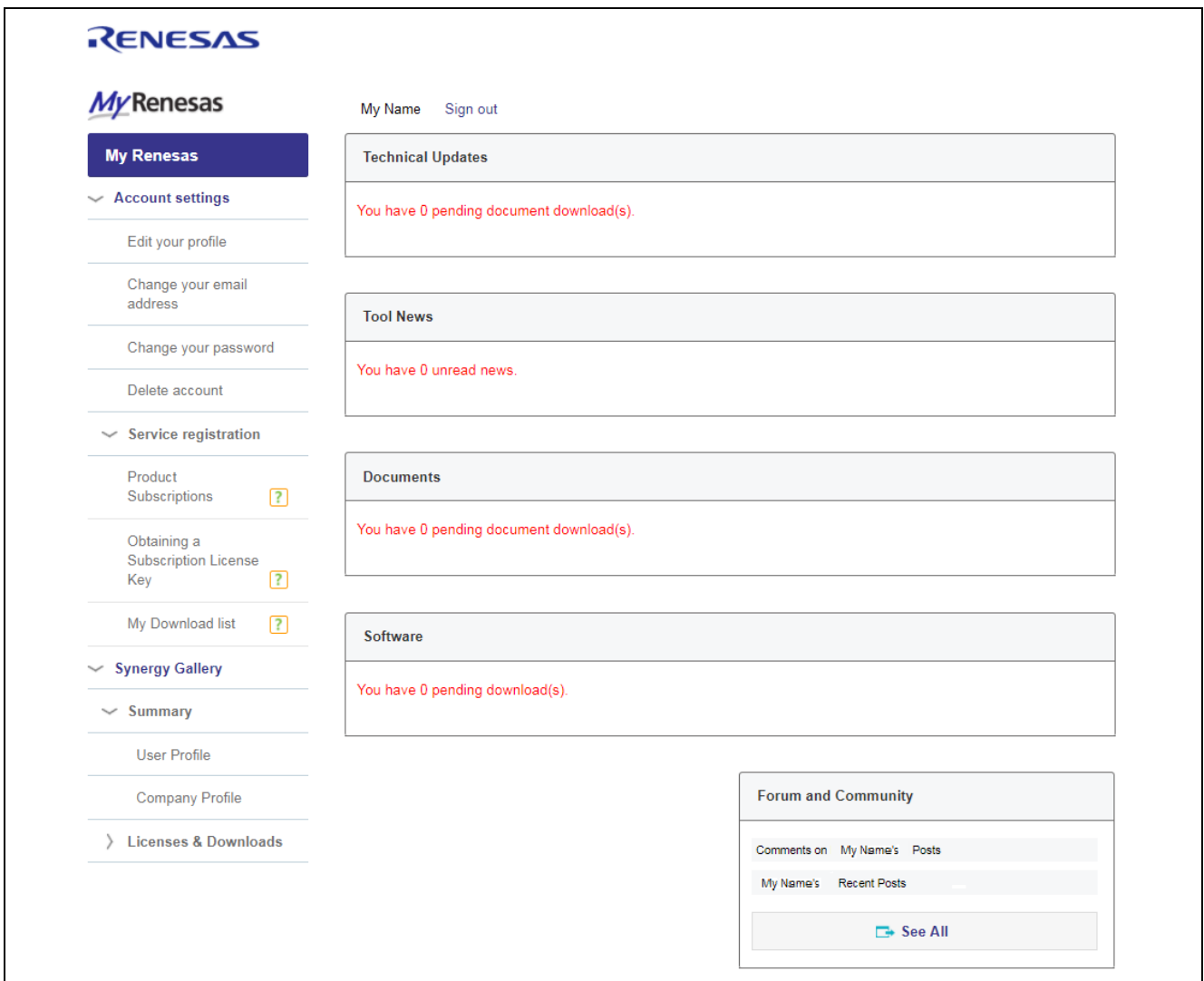
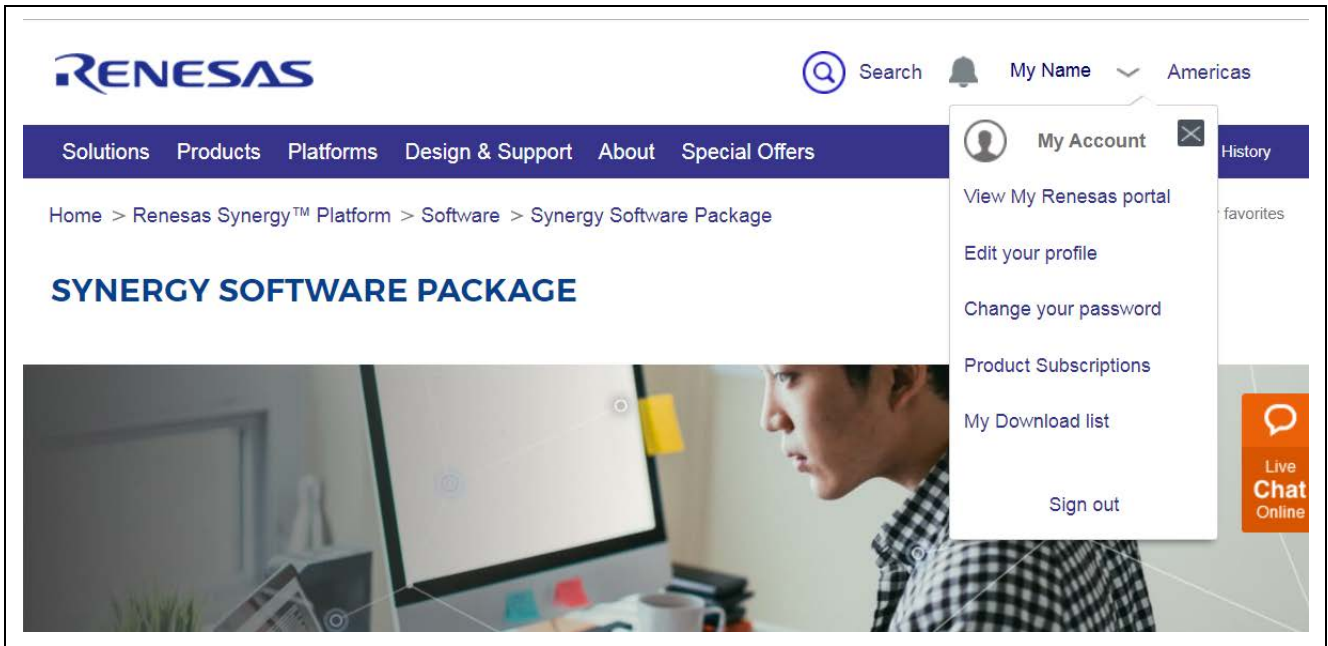
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3. S1JA MCU is currently supported by IAR EW for Synergy v8.21 or later version of toolchain. The S1JA is an Arm® Cortex® M23 which uses the Armv8-M architecture.

**Note:** Armv8-M architecture is not supported by the current version of GCC included with e<sup>2</sup> studio in this release. When creating a project, the GCC toolchain may be selected by default. If so, change it to select the IAR compiler.

For instructions on installing IAR compiler in e<sup>2</sup> studio, see the application note, *Installing IAR Compiler into e<sup>2</sup> studio*. The document is available from the e<sup>2</sup> studio downloads section, or may be accessed using <https://www.renesas.com/en-us/products/synergy/software/tools/e2-studio.html>

### 3. Synergy MCU groups supported

MCU Groups: S7G2, S5D9, S5D5, S5D3, S3A7, S3A6, S3A3, S3A1, S124, S128, and S1JA

Note: Currently, S1JA and S5D3 kits are only available for limited customer engagements.

### 4. Software Tools and Hardware Kits supported with this SSP release

Tool	Version	Description
e <sup>2</sup> studio	6.2.1	Software development and debugging tool. Link: <a href="https://www.renesas.com/en-us/products/synergy/software/tools.html">https://www.renesas.com/en-us/products/synergy/software/tools.html</a>
IAR Embedded Workbench® for Renesas Synergy™	8.23.1	Software development environment and debugging tool. Link: <a href="https://www.renesas.com/en-us/products/synergy/software/tools.html">https://www.renesas.com/en-us/products/synergy/software/tools.html</a>
SSC	6.2.1	Synergy Standalone Configurator. Used in combination with IAR EW for Synergy. Link: <a href="https://www.renesas.com/en-us/products/synergy/software/tools.html">https://www.renesas.com/en-us/products/synergy/software/tools.html</a>
GNU Arm Compiler	4.9.3	GNU Arm® compiler GCC_4.9.3.20150529
IAR Compiler	8.23.1	IAR Arm® compiler toolchain
PE-HMI1	2.0	Product Example (PE) for Human Machine Interface to evaluate Renesas Synergy™ S7G2 MCU Group
DK-S124	3.1	Development Kit for Renesas Synergy™ S124 MCU Group
DK-S7G2	3.1	Development Kit for Renesas Synergy™ S7G2 MCU Group
SK-S7G2	3.3	Starter Kit for Renesas Synergy™ S7G2 MCU Group
DK-S3A7	2.0	Development Kit for Renesas Synergy™ S3A7 MCU Group
PK-S5D9	1.0	Promotion Kit for Renesas Synergy™ S5D9 MCU Group
DK-S128	1.1	Development Kit for Renesas Synergy™ S128 MCU Group
TB-S3A6	1.0	Kit for Renesas Synergy™ S3A6 MCU Group
TB-S5D5	1.1	Kit for Renesas Synergy™ S5D5 MCU Group
TB-S5D3#	See note	Kit for Renesas Synergy™ S5D3 MCU Group
TB-S3A3	1.0	Kit for Renesas Synergy™ S3A3 MCU Group
TB-S3A1*	1.0	Kit for Renesas Synergy™ S3A1 MCU Group
TB-S1JA*	1.0	Kit for Renesas Synergy™ S1JA MCU Group
J-Link Software	6.32F	SEGGER J-Link® debug probe is the quasi standard for Arm® Cortex®-M based MCUs

Note: \* Pre-production versions of these kits were used for SSP testing; results with production kits may vary slightly.

# Target Board S5D3, Version 0.5a; Base Board S5D5, Version 0.6a

## 4.1 Version Information for Third-Party Products

Component	Version
ThreadX®	5.8 SP1
NetX™	5.9 SP5
NetX Duo™	5.10 SP5
NetX Application bundle	5.9 SP5
NetX Duo Application bundle	5.10 SP5
NetX Web HTTP/HTTPS	5.11
USBX™ Host	5.8 SP3
USBX™ Device	5.8 SP3
FileX®	5.5 SP1
GUIX™	5.4.1
LevelX	5.4
TraceX®	5.2.0
GUIX Studio™	5.4.1.1
NetX Duo Secure	5.11
MQTT for NetX Duo	5.10 SP5
SNMP for NetX	5.11
SNMP for NetX Duo	5.11
TES D/AVE 2D	3.17

## 5. SSP release package and installation information

This package contains the SSP v1.5.0 release.

Before installing SSP standalone installer, ensure that the following items are installed on your PC:

- **Renesas e<sup>2</sup> studio ISDE v6.2.1** (download and install the e<sup>2</sup> studio Installer from Renesas.com at <https://www.renesas.com/en-us/products/synergy/software.html>)
- **GNU Arm® Compiler** (included with Renesas e<sup>2</sup> studio ISDE v6.2.1)

To install the SSP, follow these steps:

1. Download the following items for the SSP Release from [Renesas.com](https://www.renesas.com):
  - **SSP\_Distribution\_1.5.0.zip** (SSP Package Installer, including SSP Package)
  - **Renesas Synergy Software Package (SSP) v1.5.0 Release Note**.
2. Unzip the package and run the **SSP\_Distribution\_1.5.0.exe installer**.
3. Install the SSP in the root folder of a compatible e<sup>2</sup> studio installation.

Note: The default installation folder for the SSP is **C:\Renesas\e2\_studio**.

SSP documentation is available for download from the Synergy Software Package (SSP) page in Renesas Synergy Platform section, on [Renesas.com](https://www.renesas.com). Sign in to the MyRenesas Account by using your existing MyRenesas or Synergy Gallery credentials, or by creating a new MyRenesas account.

## 6. Changes from SSP v1.4.0 to SSP v1.5.0 release

### 6.1 New or updated features

#### 6.1.1 Crypto/r\_sce

Added driver support for ECC P-224 and P-384 curves. This includes APIs for scalar multiplication, key generation, ECDSA signature generation, and ECDSA signature verification operations. API supports both plain-text and wrapped keys.

**Applies to:** S5 and S7 MCU Series

#### 6.1.2 DHCP Option 60

The DHCP option 60 (Vendor Class Identifier), and DHCP option 61 (Client Identifier), as well as other options, can be added for DHCP request using the registered callback.

#### 6.1.3 LevelX

NOR flash memory can only be erased a finite number of times; it's critical to distribute the flash memory use evenly. LevelX NOR provides NOR Flash Leveling support.

The LevelX NOR feature requires the LevelX NOR driver provided by the SSP framework, SF\_EL\_LX\_NOR. LevelX NOR can be used directly or with FileX. To use LevelX NOR, the flash should be erased or formatted. The write and erase times vary based on MCU type.

**Applies to:** S7G2, S5D9, S5D5, S5D3, S3A7, S3A1, and S3A3 MCU Groups

#### 6.1.4 NetX Web HTTPS Client

The HTTPS Client module provides high-level APIs for Hyper Text Transport Protocol (HTTP) used to securely transfer content on the web. HTTPS is the secure version of HTTP protocol which uses HTTP on top of Transport Layer Security (TLS) protocol to secure the underlying TCP connection.

**Applies to:** S7G2 and S5D9 MCU Group

#### 6.1.5 NetX Web HTTP1.1 Client

The NetX Web HTTP 1.1 Client module provides high-level APIs for the Hyper Text Transport Protocol (HTTP) used in transferring content on the web. The client implementation conforms to RFC 1945 "Hypertext Transfer Protocol/1.0" and RFC 2616 "Hypertext Transfer Protocol – HTTP/1.1."

**Applies to:** S7 and S5 MCU Series

#### 6.1.6 sf\_cellular

- Cellular Framework now supports fallback to EGPRS when the device is out of LTE coverage area and provides a Network Fallback sequence selection via the ISDE Configuration. The default Network Fallback sequence can be changed in ISDE.
- Custom AT commands can now be sent to the Cellular module and receive a response using the commandSend() API. If the module is in Data mode, this API handles switching to command mode to send the AT command.
- Cellular framework supports NB-IoT for Quectel BG96. To connect to the NB-IoT network, the user should set the Scan sequence to LTE Cat.NB1->LTE Cat.M1->GSM in the properties for Quectel BG96.
- Cellular framework enables the application to capture the AT command/response communication between the cellular framework and module.

**Applies to:** Cellular Framework on all MCUs

#### 6.1.7 sf\_el\_fx

If sector release is enabled by the driver during initialization, FileX informs the driver whenever one or more consecutive sectors become free. If the driver is a FLASH manager, FileX can tell the FLASH manager that these sectors are no longer needed. FLASH manager will then free-up the sectors for future use.

**Applies to:** All the MCUs with FileX support.

#### 6.1.8 nxd\_tls\_secure

- Added support for TLS1.1 and MD5
- Added support for RSA 4096 Software crypto

**Applies to:** All the MCUs with TLS support

## 6.2 New Improvements

### 6.2.1 Express Logic Component Integration into SSP

The following Express Logic modules have been upgraded:

- NetX v5.9 SP5, NetX Duo v5.10 SP5
- NetX Application bundle v5.9 SP5, NetX Duo Application bundle v5.10 SP5
- FileX v5.5 SP1
- ThreadX v5.8 SP1
- MQTT for NetX Duo v5.10 SP5
- LevelX v5.4
- USBX Host v5.8 SP3, USBX Device v5.8 SP3
- GUIX v5.4.1, GUIX Studio v5.4.1.1
- NetX Web HTTP/HTTPs v5.10

### 6.2.2 r\_cgc

**Issue ID:** 10101

Options in the CGC configuration block have been limited to those available for each MCU.

**Applies to:** All MCUs

### 6.2.3 r\_qspi

**Issue ID:** 6612

Multiple-line page program is now supported. Existing projects require modification to the `bsp_qspi.h` header file to take advantage of this feature. Page programming by default uses only one line (D0). To use multiple lines during page program, define the command as one of the following macros in `bsp_qspi.h`:

`QSPI_COMMAND_PAGE_PROGRAM_QUAD`,  
`QSPI_COMMAND_4BYTE_PAGE_PROGRAM_QUAD`,  
`QSPI_COMMAND_PAGE_PROGRAM_DUAL`, or  
`QSPI_COMMAND_4BYTE_PAGE_PROGRAM_DUAL`.

Also, define `QSPI_PAGE_PROGRAM_ADDRESS_ONE_LINE` to 1, if the address should be sent on D0 only during multiple line program commands. An example can be found in `bsp_qspi.h` for DK-S7G2, starting in SSP version 1.5.0.

**Applies to:** S7G2, S5D9, S5D5, S5D3, S3A7, S3A3, S3A1 MCU Groups

### 6.2.4 r\_riic

**Issue ID:** 11995

"Read-modify-write" is performed to clear the next interrupt status flags. Software is modified to clear the flags, according to the specification, to avoid future issues.

**Applies to:** All MCUs

### 6.2.5 sf\_audio\_playback

**Issue ID:** 11433

When playing 8-bit audio data, chunks of data were skipped. This occurs when the data packet size is less than the size of the internal audio buffer and data processing is required, or when the data packet is larger than the internal audio buffer. This issue is fixed and 8-bit audio samples can now be played on a lower level driver that requires 16-bit samples. The samples are converted from 8-bits to 16-bits in the audio playback framework.

**Applies to:** All MCUs

### 6.2.6 sf\_cellular

**Issue ID:** 12462

After calling Cellular framework open(), application can use the Custom AT command sending API to send AT commands to the module. This allows the application to perform custom settings on the module after the open().

**Applies to:** Cellular framework on all Synergy MCUs

**Issue ID:** 12497

Cellular framework now supports BG96 RAK Wireless WisLTE Rev F\* boards

**Applies to:** Cellular framework for Quectel BG96 on S5D9 and S7G2 MCU Groups

**Issue ID:** 11322

Cellular framework common implementation now takes the reset polarity from the configurator options.

**Applies to:** Cellular framework on all Synergy MCUs

**Issue ID:** 12498

Updated the networkStatusGet API in Cellular framework to provide Access Technology details and registration details (Home, Roaming, or Not registered).

**Applies to:** Cellular framework on all Synergy MCUs

### 6.2.7 sf\_el\_nx\_comms

**Issue ID:** 6532

The sf\_el\_nx\_comms module does not support dual Ethernet connections. Use sf\_comms\_telnet in new designs or migrate the old projects to sf\_comms\_telnet as sf\_el\_nx\_comms is not supported.

**Applies to:** S7G2, S5D9, and S5D5 MCU Groups

### 6.2.8 sf\_touch\_panel\_v2

**Issue ID:** 11104

SF\_TOUCH\_PANEL\_V2 SSP framework is implemented. Refer to module usage notes for details.

### 6.2.9 TES D/AVE 2D driver

**Issue ID:** 9566

The d2\_utility\_fbblitcopy utility function uses a wrong wait command to sync framebuffer reads and writes. The wait command waits only for the pipeline to finish, but it should wait for all caches being flushed. The TES D/AVE 2D driver v3.17 resolves this issue.

**Applies to:** S7G2 and S5D9 MCU Groups

### 6.2.10 USBX

**Issue ID:** 10102

The USBX DEVICE HID CLASS was used to support only a single interface (keyboard or mouse). Now USBX DEVICE HID CLASS supports a multi-interface configuration (keyboard + mouse simultaneously).

**Applies to:** All MCUs

## 7. Issues Fixed since 1.5.0-rc.1 release

### 7.1 BSP for SSP Supported Platforms

**Issue ID:** 12049

The default values for the MPU regions have been fixed to not overlap multiple sections.

**Applies to:** S1JA, S128, S3A1, S3A3, S3A6, S5D3, S5D5, S5D9 MCU Groups

### 7.2 Crypto/r\_sce

**Issue ID:** 12719

SignFinal API can be called if the overall message accumulated after one or more calls to signUpdate followed by signFinal OR signFinal Only, is less than the desired HASH size, as specified in the message\_format.

This issue is also fixed for Signature Verify.

**Applies to:** S5 and S7 series MCUs

**Issue ID:** 12617

The endianness is configurable in ISDE. Both HAL R\_SCE and TLS sf\_el\_nx\_crypto modules will use that endianness configuration.

It is recommended that little endian be used with TLS stack.

Note: Existing projects using TLS alone are required to set the r\_sce common driver property of Endian flag to CRYPTO\_ENDIAN\_LITTLE to maintain backward compatibility.

**Applies to:** S7G2, S5D9 MCU Groups

**Issue ID:** 12928

The module descriptor file of r\_sce module is updated, which allows the user to use the following Crypto HAL modules in the user application project:

- AES - 192-bit support on all chaining modes (ECB, CBC, CTR, GCM)
- ARC4
- DSA
- ECC
- HASH
- RSA
- TDES

sf\_crypto\_hash and sf\_crypto\_signature framework modules using the r\_sce\_hash HAL module will also be usable.

**Applies to:** S5D3 MCU Group

### 7.3 NetX

**Issue ID:** 12663

Build failure caused by incorrect generated codes by NetX Duo FTP server when used with IPv6 disabled has been fixed.

**Applies to:** S7G2, S5D9, S5D5 MCU Groups

**Issue ID:** 12272

With latest NetX and NetX Duo SNMP, the limitation to set IP addresses with the most significant byte/octet greater than 127 has been resolved. Now user can set any valid IP address.

**Applies to:** All MCU/boards which support NetX and NetX Duo SNMP

**Issue ID:** 12197

There are xml configuration properties like NX\_SNMP\_MAX\_TRAP\_NAME, NX\_SNMP\_TIME\_INTERVAL, which are not in use. The xml file is now modified to remove these properties from the configurator. So, these properties will not be displayed.

**Applies to:** All MCUs

**Issue ID:** 13011

The issue of TCP Socket cleanup in case of tls\_setup callback failure is fixed in NetX Duo Web HTTP v5.11.

**Applies to:** S7G2, S5D9, S5D3, S5D5 MCU Groups

**Issue ID:** 12915

Web HTTP client 5.11 now supports chunked encoding feature as described in RFC 2616.

**Applies to:** S7G2, S5D9, S5D5 MCU Groups

**Issue ID:** 12997

The SDMMC open() API returned an error when 8-bit eMMC was selected and parameter checking was enabled. This is fixed.

**Applies to:** S7G2, S5D9, S5D5, S3A7, S3A6, S3A3, S3A1 MCU Groups

## 7.4 nxd\_tls\_secure

**Issue ID:** 12726

The meta data buffer size is a user-supplied field; information about it can already be found in EL NetX secure usage guide and Renesas usage guide. Before the TLS session is created, the meta data buffer must be allocated. The size of meta data can be set using the properties pane.

Due to addition of RSA 4k decode feature in software, the default value of meta data buffer needs to be increased using the properties pane only if the application is using the maximum modulus size to be 4k.

**Case 1:** Microsoft Azure server certificate, which is signed by 4K bit key needs larger meta buffer size. In such a case, the user should increase the meta buffer size from its default value of 4k. For such a case, the user should ensure that following properties in the pane are set as shown below.

Meta buffer size: 16000 (user should change value from 4000 to 16000)

Maximum modulus size in bits: 4k (default, no change)

**Case 2:** Amazon AWS server certificate, which is signed by 2K bit key can sufficiently use default value of 4000 for meta buffer size. For such a case, the user should ensure that the following properties in the pane are set as follows:

- Meta buffer size: 4000 (default, no change)
- Maximum modulus size in bits: 2k (user should change value from 4k to 2k)

In summary, the user needs to adjust meta buffer size or maximum modulus size in bits according the length of key used by the server.

Recommendation: The application needs to change "meta buffer size" or "Maximum modulus size" depending on the requirement.

**Applies to:** S7G2, S5D9 MCU Groups

## 7.5 r\_dac

**Issue ID:** 12661

Synergy configurator is updated to disable output amplifier for r\_dac module on S1JA MCU since S1JA does not support output amplifier.

**Applies to:** S1JA MCU Group

## 7.6 r\_flash\_hp

**Issue ID:** 12670

Updated linker script so new projects will have code linked in an allowed region of memory. Added run time check to verify code address for migrated projects. Documentation has been added to indicate how to update migrated projects if functions are being linked in an invalid location.

**Applies to:** S5 Series MCUs

**Issue ID:** 12652

When using r\_flash\_hp, the flash access window cannot be set to include the last block. This issue is now fixed.

**Applies to:** S5 and S7 Series MCUs

## 7.7 r\_riic

**Issue ID:** 12209

The r\_riic master driver was not aborting when error events (timeout/NACK) occur at the end of transfer. The issue is now fixed by updating the r\_riic master driver by updating the err flag to capture error events and abort the transfer by returning the error.

**Applies to:** All the MCUs

## 7.8 r\_sdadc

**Issue ID:** 12611

The generated configuration code is now properly referenced in XML for channel 1 and this channel can be configured during open.

**Applies to:** S1JA MCU Group

## 7.9 sf\_cellular

**Issue ID:** 12656

The framework now has a provision in the ISDE to increase this polling attempt to greater than 25. This will allow the framework to poll for a longer time on some networks that need more time to register the module.

**Applies to:** Cellular framework

## 7.10 sf\_console

**Issue ID:** 13035

If the mutex is not released when the error condition `SSP_ERR_OVERFLOW` occurs, any subsequent calls to the module will fail. So, the mutex must be unlocked before returning out of `sf_console_read_main()`.

**Applies to:** All MCUs

**Issue ID:** 9443

The `SF_CONSOLE_Read` API returns an error value, `SSP_ERR_OVERFLOW`, if the `NULL` value is passed for parameter `p_dest`.

**Applies to:** All MCUs

**Workaround:** None

## 7.11 sf\_crypto

**Issue ID:** 12421

Auto init property for `sf_crypto` will now work based on user selection.

**Applies to:** All MCUs

## 7.12 sf\_el\_ux\_comms\_v2

**Issue ID:** 12757

Previously, in case of write/read failure using `sf_el_ux_comms_v2` framework, the subsequent call to the comms framework write/read caused an indefinite hang. This is due to the thread object (Mutex) not being released in case of write/read failure. This issue has been fixed in this release.

**Applies to:** All Synergy MCU Groups

## 7.13 SSP IAR Support

**Issue ID:** 11842

Hardware reset has been increased to 400 to allow debugger to wait for additional time before communicating with the device.

**Applies to:** DK-S7G2, PE-HMI



## 8. Summary of bug fixes in SSP v1.5.0-rc.1

### 8.1 BSP for SSP supported Platforms

**Issue ID:** 7619

Changed the default pin configuration for PB06 from ETH WOL to GPIO active-high.

**Applies to:** PE\_HMI board

**Issue ID:** 7763

There previously existed a condition in which a circuit that is not used in user mode might not reset and could operate in an unstable state due to the clocks not being supplied during a reset of an MCU. This condition could result in the supply current increasing to a value greater (by up to 600  $\mu$ A) than stated in the User's Manual when the MCU transitions to Low-Speed mode or to the Software Standby mode. This issue has now been resolved.

**Applies to:** S1 and S3 MCU Series

**Issue ID:** 8650

The Snooze Cancel event signal, ELC\_EVENT\_ICU\_SNOOZE\_CANCEL, is now available for use on S3A3 MCUs in bsp\_elc.h.

**Applies to:** S3A3 MCU Group

**Issue ID:** 8651

The GPT UVW Edge event signal, ELC\_EVENT\_OPS\_UVW\_EDGE, is now available for use on S3A3 MCUs in bsp\_elc.h.

**Applies to:** S3A3 MCU Group

**Issue ID:** 9104

Fixed the monitored region for the main stack to not include the thread stacks when using GCC. Note that the address of symbol \_\_StackTop has changed to be the top of the main stack. Existing projects should modify the linker to match the following script:

```
/* Stacks are stored in this section. */
stack_dummy (NOLOAD):
{
= ALIGN(8);
__StackLimit = .;
/* Main stack */
KEEP(*(.stack))
__StackTop = .;
/* Thread stacks */
KEEP(*(.stack*)) .
__StackTopAll = .;
} > RAM
PROVIDE(__stack = __StackTopAll);

/* This symbol represents the end of user allocated RAM. The RAM after this
symbol can be used ...at run time for things such as ThreadX memory pool
allocations.
*/ __RAM_segment_used_end__ = ALIGN(__StackTopAll , 4);
```

**Applies to:** All MCUs using the GCC compiler; except for S7G2

## 8.2 Crypto/r\_sce

**Issue ID:** 11206

For ECC 192/256-bit Key generation operations, users were restricted to input exact key data buffer length and were not allowed to input key data buffer length which is greater than key length. This is fixed by allowing buffer length to be equal or greater than the length of the generated key.

For ECC scalar multiplication operation, Scalar point buffers were allowed with equal or more data lengths. This is fixed by requiring the length of input key buffers to be exactly equal to the key lengths used. Also, the output buffer can be greater than or equal to the length of the expected output data.

**Applies to:** S5 and S7 MCU Series

**Issue ID:** 12230

The ECDSA signature verification APIs are fixed and now return the appropriate error code when zeroes are entered as the signature.

**Applies to:** S5 and S7 MCU Series

**Issue ID:** 12408

A new KeyInstall2() API is introduced in the HAL Library through the key\_installation module. The format of the RSA wrapped key generated in the HAL key\_installation module, as the output of the keyInstall2 API is the same as the one the HAL RSA module/keyCreate API outputs. The RSA modulus is concatenated to the private, wrapped exponent. The API is compatible with all other Crypto APIs.

**Applies to:** All S5 and S7 MCU series that support RSA Key Installation

## 8.3 GUIX Driver Work

**Issue ID:** 11518

Characters were not rendered properly on the LCD, if the CLUT8 format and D/AVE 2D were used in the application. This issue is fixed in D/AVE 2D.

**Applies to:** S7G2 and S5D9 MCU Groups

**Issue ID:** 12439

Incorrect code was being generated from GUIX Studio 5.4.0 when a template is used. The issue has been fixed with GUIX Studio 5.4.1.1.

**Applies to:** S7 and S5 MCU Series

## 8.4 GUIX

**Issue ID:** 11712

An incorrect definition was provided for gx\_scroll\_wheel\_selected\_get and gxe\_scroll\_wheel\_selected\_get in the gx\_api.h.

The issue has been fixed by providing proper definitions for the gx\_scroll\_wheel\_selected\_get and gxe\_scroll\_wheel\_selected\_get in the gx\_api.h.

**Applies to:** S7G2 and S5D9 MCU Groups

## 8.5 NetX

**Issue ID:** 10152

SNTP Client time update functions properly as its polling interval has been configured less than its maximum time adjustment.

**Applies to:** S7G2, S5D9, and S5D5 MCU Groups

**Issue ID:** 11132

NetX IP instance internal stack memory allocation is ensured to be 8-byte aligned in accordance with the Arm® EABI interface.

**Applies to:** S7G2, S5D9, and S5D5 MCU Groups

## 8.6 nxd\_mqtt\_client

### Issue ID: 10572

MQTT client fails when a second client running on a different board with the same ID is connected to the same broker. In this case the first client reports an error. The error returned by first client is NXD\_MQTT\_NOT\_CONNECTED (0x10002 - the client is not connected to the broker).

After the first client is unable to establish a secure connection with the broker, the second client remains securely connected to the broker.

The fix ensures that the application creates unique MQTT client id. The MQTT usage note has an example on how to create a unique MQTT client id.

**Applies to:** S5D9 and S7G2 MCU Groups

### Issue ID: 10573

MQTT client configurator allows the user to configure the maximum length of topic using "Topic Name Max Length" property.

If a MQTT client subscribes to a MQTT topic whose length is more than maximum configured topic length, the nxd\_mqtt\_client\_subscribe()/nxd\_mqtt\_client\_publish() API does not return an error.

The implementation of nxd\_mqtt\_client\_subscribe()/nxd\_mqtt\_client\_publish() API has been modified in MQTT 5.10SP5 and fixes this issue. Now, if the length of topic\_names passed to nxd\_mqtt\_client\_subscribe()/nxd\_mqtt\_client\_publish() APIs exceeds the configured MAX\_TOPIC\_NAME\_LENGTH, then the API returns an error.

**Applies to:** S7G2 and S5D9 MCU Groups

### Issue ID: 10581

MQTT API nxd\_mqtt\_client\_secure\_connect() used to hang when the MQTT client tried to reconnect to a MQTT broker after performing standard MQTT operations, such as a publish/subscribe operation. This issue is now fixed.

**Applies to:** S7G2 and S5D9 MCU Groups

### Issue ID: 11348

NetX Duo MQTT Client had a bug that prevented multiple MQTT Clients from running on the same device.

This issue has been traced down to the use of a global variable in the MQTT code. This issue is fixed in MQTT 5.10SP5.

**Applies to:** S5D9 and S7G2 MCU Groups

### Issue ID: 12219

A memory corruption exists under certain conditions. The cause is repeated use of nxd\_mqtt\_client\_publish() or nxd\_mqtt\_client\_subscribe() public APIs by the application.

The memory corruption issue is fixed by ensuring that APIs return an error if the topic name passed to them is greater than max topic length. In particular, nxd\_mqtt\_client\_publish()/nxd\_mqtt\_client\_subscribe() APIs return an error if the length of the topic\_name passed to them exceeds the maximum topic name length.

**Applies to:** S5D9 and S7G2 MCU Groups

### Issue ID: 9915

MQTT server closes the connection if the first message received by the server is PUBLISH or SUBSRIBE, and the packet identifier field in the received message is zero. A fix is put in place to ensure that packet identifier is set to non-zero value.

**Applies to:** S5D9, S7G2 MCU Groups, and Azure IoT hub.

## 8.7 nxd\_tls\_secure

### Issue ID: 10639

The TLS client is unable to establish a secure connection using TLS protocol to server renesas.dweet.io. The client cannot establish secure connection due to mismatch in expected size of the public exponent field of the root certificate received from the server. The client expects the size of the public exponent field to be 3 bytes, whereas the server sent 1-byte public exponent field in its certificate.

The issue is fixed by having the RSA driver accept exponent size equal to 1 or 2 bytes.

**Applies to:** S5D9 and S7G2 MCU Groups

**Issue ID:** 10691

When the device is in HTTPS server mode, the desktop based HTTPS client (such as the browser) pauses so the desktop user can add a certificate exception. Up to the time the user does not add any certificate exception, the client won't send any packets to the server. In these instances, the `nx_secure_tls_session_receive()` returns an error on the server side. If the server application does not check for a return value and continues to process packets regardless of the error indicated earlier, this issue causes the SSP to hang.

The fix is to check the return value of the API `nx_secure_tls_session_receive()`. If the API returns an error, do any clean up needed (such as disconnecting the socket and so on), and then continue.

**Applies to:** S5D9 and S7G2 MCU Groups

**Issue ID:** 10738

If the two TLS instances are used, the first one can establish connection, works fine and can be deleted afterwards. However, an attempt to establish connection using the second TLS instance does not work. This issue was traced to a leaky mutex and thus the second TLS instance hung.

This issue was fixed by Express Logic in NetX Secure 5.11.

**Applies to:** S5D9 and S7G2 MCU Groups

## 8.8 `r_acmplp`, `r_acmphs`

**Issue ID:** 11600

When using either comparator driver (`r_acmphs` or `r_acmplp`), the interrupt was not mapped into the vector table in the generated code. This is fixed.

**Applies to:** S1JA MCU Group

## 8.9 `r_agt`

**Issue ID:** 11098

In a cascaded timer setup, where the output of the first timer T0 is input to a second timer T1:

1. Clock dividers in the configuration of timer T0 are considered in the calculation of input frequency of timer T1.
2. The calculation of T1 count value is modified such that the accuracy of the output frequency of timer T1 is improved with the granularity of  $1/T1$  source frequency.

**Applies to:** All MCUs

## 8.10 `r_cgc`

**Issue ID:** 12360

Resolves a bug where switching to the sub-clock oscillator, from the internal high-speed oscillator or mid-speed oscillator, did not enable Low-Power mode.

**Applies to:** All MCUs

**Issue ID:** 10697

The PLL multiplier values of 8 and 9 are included in the configuration properties displayed and can be selected for S3 MCU Series.

**Applies to:** S3 MCU Series

**Issue ID:** 10698

Support to choose optimum power control mode based on the selected system clock is added to the `SystemClockSet()` function in the `r_cgc` module.

**Applies to:** All MCUs

**Issue ID:** 10700

The CGC driver allows transition from High-Speed mode to Sub-Oscillator-Speed mode.

**Applies to:** All MCUs

**Issue ID:** 10810

Configurator gives the correct option to select the clock source for PLL.

**Applies to:** All MCUs, except S1 series

**Issue ID:** 10832

Using a peripheral clock on any unsupported MCU will now return an error. The `R_CGC_SystemClockFreqGet ()` API now returns `SSP_ERR_INVALID_ARGUMENT` for unsupported peripheral clocks.

**Applies to:** All MCUs

**Issue ID:** 8578

If an attempt is made to set an inactive (LOCO/MOCO) clock as a system clock, the driver now returns an error. To set a system clock correctly:

1. Start the desired clock.
2. Set the clock as the system clock.

**Applies to:** All MCUs

## 8.11 r\_dac

**Issue ID:** 7797

The Synergy Configuration Tool for `r_dac` allows configuration of the Output Amplifier for S3A7, S3A3, and S124 MCU Groups, even though these MCUs do not have an output amplifier. The output amplifier setting is disabled on these MCUs since it has no effect.

**Applies to:** All MCUs

## 8.12 r\_flash\_hp

**Issue ID:** 11425

`UpdateFlashClockFreq` now returns an error if called while an operation is in progress.

**Applies to:** S5 and S7 MCU Series

## 8.13 r\_flash\_lp

**Issue ID:** 11424

`UpdateFlashClockFreq` now returns an error if called while an operation is in progress.

**Applies to:** S1 and S3 MCU Series

**Issue ID:** 11593

`R_FLASH_LP` driver writes ones (1s) to the unused bits in the AWSC register.

**Applies to:** S1 and S3 MCU Series

`R_FLASH_HP` driver writes ones (1s) to the unused bits in the AWS register and the unused words surrounding AWS.

**Applies to:** S5 and S7 MCU Series

## 8.14 r\_glcd

**Issue ID:** 9226

A hardware technical note was issued for the GLCD peripheral. The technical note impacts the `R_GLCD` HAL driver and following issue was identified.

The very first Line Detect Interrupt could happen at unexpected timing. Normally the interrupt would happen at the timing when the GLCDC peripheral goes into the blanking period (front porch). This issue would impact to customers who uses the Line Detect Interrupt for the timing to update a LCD screen. The GLCD driver was updated as per the technical note

**Applies to:** All MCUs

## 8.15 r\_gpt

**Issue ID:** 11230

GPIO requires  $1/PCLD$  time to generate one PWM cycle. So, the ON time is always  $((DutyCycle\ value + 1) / PCLD)$ . Added is a new configuration property that enables low duty cycle raw counts (1 PCLK) and updates the driver to set the duty cycle in PWM mode.

**Applies to:** All MCUs

## 8.16 r\_ioport

**Issue ID:** 11694

The R\_IOPORT\_PinEventOutputWrite() API was writing (set/clear) on the whole port, which is now updated to write (set/clear) a value for the dedicated pin on a port.

**Applies to:** All MCUs

## 8.17 r\_lpmv2

**Issue ID:** 12231

The LPM V2 module enters module-stop for modules before entering standby. Entering module-stop is necessary to prevent a large change in operating current causing undefined behavior in the MCU.

**Note:** These peripherals (ETHERC, EPTP, SCE, DRW, JPEG, GLCDC, and GPT) remain in a stop state during the interrupt that wakes the device from Standby mode. The peripherals start again by the time lowPowerModeEnter returns.

**Applies to:** S5D9, S5D5, and S5D3 MCU Groups

## 8.18 r\_lvd

**Issue ID:** 10714

LVD voltage monitor 1 and 2 values can now be displayed in configurations as per the selected MCU.

**Applies to:** All MCUs

## 8.19 r\_riic

**Issue ID:** 11091

The issue of missing TEI interrupt when TXI interrupt is getting delayed due to serving the other higher priority interrupts or running the critical section of code is now resolved.

**Applies to:** All MCUs

**Issue ID:** 11342

When the STOP condition detection interrupt (SPIE) was enabled, it caused unexpected interrupts in the Synergy I<sup>2</sup>C slave device, even when the Stop condition was meant for another device on the bus. To prevent such unintended interruption, I<sup>2</sup>C slave SPIE is now enabled only after Receive Data Full Flag (RDRF) or Transmit Data Empty Flag (TDRE) is true to ensure that the call-back occurs only if the Stop condition is meant for this slave.

**Applies to:** All MCUs

**Issue ID:** 12393

When close API is called while transfer is in progress, the API returns SSP\_ERR\_ABORTED without actually closing the driver.

This issue is fixed by removing all the error return checks after riic\_abort\_seq\_master() function call —and checking it after riic\_close\_hw\_master() function call. Now, the driver closes successfully and returns SSP\_ERR\_ABORTED.

**Applies to:** All MCUs

**Issue ID:** 8592

RIIC peripheral, during a clock stretch by the communicating device, supports timeout error with two timeout values (SHORT and LONG). RIIC driver was configuring the timeout value to SHORT mode and was not providing an option for the user to change it.

The driver and configurator for RIIC was modified to provide the user with the option to set the timeout mode in case of a clock stretch. The default configuration option is set to SHORT mode, to allow for backward compatibility.

**Applies to:** All MCUs

**Issue ID:** 9734

Updated the RIIC driver to wait until the bus is free after the transfer is completed when using callback and in blocking method.

**Applies to:** All MCUs

## 8.20 r\_rspi

**Issue ID:** 12078

TXI interrupt was being disabled in the NVIC. It is now disabled in the RSPI peripheral too. Any pending ICU/NVIC interrupts are also cleared

**Applies to:** All MCUs

## 8.21 r\_rtc

**Issue ID:** 11096

The calenderAlarmSet API forcefully modified the periodic IRQ rate to RTC\_PERIODIC\_IRQ\_SELECT\_1\_DIV\_BY\_64\_SECOND. This issue is fixed.

**Applies to:** All MCUs

**Issue ID:** 11404

R\_RTC driver had a bug where the user sometimes missed a carry event callback when the calenderTimeGet API was in progress. This issue is fixed.

**Applies to:** All MCUs

**Issue ID:** 11595

The calenderCounterStart and calenderCounterStop APIs did not wait for the start bit change to be reflected in the register. This issue caused the infoGet API to return an incorrect status if called immediately after a start/stop API. This issue is fixed.

**Applies to:** All MCUs

**Issue ID:** 12006

IRQ bits of RTC peripheral were not disabled during module close, which caused an IRQ state to be pending. This issue immediately triggered when the module was reopened and the IRQs enabled. Also, the irqEnable API did not clear any pending IRQ before enabling the IRQ. These issues are fixed.

**Applies to:** All MCUs

## 8.22 r\_sci\_i2c

**Issue ID:** 7946

SCI I<sup>2</sup>C master driver, when used without DTC (when the driver operates in CPU interrupt mode), was causing a glitch on the I<sup>2</sup>C bus. The glitch was observed between the generation of the START condition and issuing of the address bits. This issue caused some I<sup>2</sup>C slaves (susceptible to high frequency noise) to NACK the address bits, causing a communication failure.

The driver was modified so it no longer causes glitches when operating without DTC support.

**Applies to:** All MCUs

## 8.23 r\_sci\_spi

**Issue ID:** 11080

Incomplete information is present in the function header of an Open, Read/Write API, and the function header of the r\_sci\_spi\_transfer\_reset and r\_sci\_spi\_tx\_transfer\_reset function was missing.

This fix updates incomplete information in function header of Open and Read/Write APIs with following information:

1. The Open API of r\_sci\_spi returns SSP\_ERR\_INVALID\_ARGUMENT if DTC instance is used for data reception but not used for transmission or vice versa.
2. The Read and Write APIs of r\_sci\_spi returns SSP\_ERR\_ASSERTION if length of data to be transmitted is more than 0xFFFF unsigned.

The missing function header of r\_sci\_spi\_transfer\_reset and r\_sci\_spi\_tx\_transfer\_reset has been updated.

**Applies to:** All MCUs

**Issue ID:** 11525

SPI transfer rate is reduced to half when bit rate modulation is enabled for certain system clock rate setting changes but when bit rate modulation is not enabled SPI transfer rate does not get impacted even if system clock rate is changed. The issue is with the register MDDR setting which takes values from 128 to 255 and not 128 to 256. This is now corrected and now changing the clock rate does not impact the transfer rate.

**Applies to:** All MCUs

**Issue ID:** 11591

After completion of data transmission, the TXI interrupt was being disabled in the peripheral. Because of this issue, two TXI and two TEI interrupts were generated after data transfer completion at higher bit rates.

Now, when data transmission is completed, and TXI interrupt is being disabled in the peripheral, then an IR bit corresponding to TXI interrupt is being cleared in ICU and the pending TXI interrupt request is being cleared in NVIC. The fix results in one TXI and TEI after transmission completion.

**Applies to:** All MCUs

## 8.24 r\_sdmmc

**Issue ID:** 10382

The r\_sdmmc driver now has the capability to disable card detection during initialization. By default, the card detection option uses the CD pin to detect presence of media, but this is not valid for eMMC. For the fix, a constraint has been added in the XML, which pops up following error message “when the Media type is Embedded, Card detection must be not used.”

**Applies to:** S7G2, S5D9, S5D5, S5D3, S3A7, S3A3, and S3A1 MCU Groups

**Issue ID:** 11177

If MCU package (such as S5D9 in LQFP-144/CFB package) does not have write protect pin, the driver was returning SSP\_ERR\_CARD\_WRITE\_PROTECTED error. The user can now configure the new configuration property in the XML to select the "Write Protection" option as "Not Used" and use the SDMMC driver with MCU packages.

**Applies to:** S7G2, S5D9, S3A7, S3A3, and S3A1 MCU Groups

## 8.25 r\_ssi

**Issue ID:** 11884

The audio playback framework would hang when used with SSI if the TXI interrupt is not serviced before a transmit underflow occurs. This is fixed.

**Applies to:** S3, S5, and S7 MCU Series

**Issue ID:** 11885

Samples were skipped if the system word length is 32 bits for a data word length of 8 bits or 16 bits, or if the system word length is 16 bits and the data word length is 8 bits. This issue caused the audio to play faster. This issue is fixed.

**Applies to:** S3, S5, and S7 MCU Series

**Issue ID:** 11886

Audio Clock Frequency (Hertz) minimum frequency in the Synergy Configuration tool was off by a factor of 2. The description is now correct.

**Applies to:** S3, S5, and S7 MCU Series

## 8.26 sf\_adc\_periodic

**Issue ID:** 11213

S3 and S1 series MCUs do not support Individual Sample and Hold mask feature. When enabled, the ADC fails to initialize and returns an error. Hence, XML changes were made in Sample and Hold Mask property. This fix made the user aware of the functionality in S3 and S1 MCU Series, while configuring r\_adc driver properties in configuration window.

**Applies to:** S3A7, S3A3, S3A1, S3A6, S124, S128, and S1JA MCU Groups



## 8.27 sf\_audio\_playback

**Issue ID:** 11504

If audio data was not fed to the audio playback framework fast enough, the audio playback framework could skip chunks of data. This issue is fixed.

**Applies to:** All MCUs

## 8.28 sf\_audio\_record

**Issue ID:** 12533

The data buffer for audio i2s record framework is declared in the thread's header file by code generator. This is in addition to the declaration elsewhere in the same XML. This results in build failure for the module, due to duplicate definition, while using IAR. This issue was fixed by addressing the duplicate definition.

**Applies to:** All MCUs

## 8.29 sf\_ble

**Issue ID:** 10375

An auto-initialization feature is provided for the BLE Framework. The application does not hang, even if the PMOD BLE module is not connected.

**Applies to:** RL78G1D BLE module on all Synergy MCUs

## 8.30 sf\_cellular

**Issue ID:** 11180

Updated AT command so that it will not reset the module while setting full functionality mode.

**Applies to:** Cellular Framework for NimbeLink CAT3

**Issue ID:** 11205

On-chip networking stack on cellular modem can transfer a maximum of 1500 bytes at a time over the socket. The cellular framework BSD socket send() and sendto() APIs restrict the maximum payload to 1500 bytes. While sending data using send() and sendto() APIs, the application should send data in chunks of 1500 bytes or less.

**Applies to:** Cellular framework BSD socket

**Issue ID:** 11224

Added response wait time for each AT command as per Cellular module AT command manual.

**Applies to:** Cellular framework for NimbeLink CAT3, NimbeLink CAT1, and Quectel BG96 module

**Issue ID:** 11590

The GetNetworkStatus API implementation is now corrected. It should now return the operator name in String format.

**Applies to:** Cellular Framework for Quectel BG96 CAT M1

## 8.31 sf\_console

**Issue ID:** 10017

Providing an up arrow key and then an enter key in the console command does not execute the previous command. This issue is fixed by adding a lock inside sub function "sf\_console\_read\_process\_up\_arrow" in the framework.

**Applies to:** All MCUs

**Issue ID:** 10386

Errors that occur during sf\_console\_read\_process\_byte are updated when an echo is enabled and the transmission unlock succeeds. The function then returns SSP\_SUCCESS, even though sf\_console\_read\_process\_byte has failed. The error variable is updated by transmission unlock before handling previous errors. The fix adds an error return check statement before it is updated by the Unlock API of sf\_comms, if the echo is enabled to avoid the update of the error variable.

**Applies to:** All MCUs

**Issue ID:** 11299

The `sf_console prompt()` API was returning `SSP_ERR_TIMEOUT` if a carriage return (CR) is received before any other character. An update handles the error code returned when `sf_console_prompt()` API receives an input string with 0 length. The error code comes from underlying `sf_comms` module and will be `SSP_ERR_TIMEOUT` for SSP `sf_comms` implementations.

**Applies to:** All MCUs

**Issue ID:** 11532

Commands such as `CMD`, `CMDHELP`, `CMD-HELP`, and `CMD_HELP` were all treated as one command only. Command parser is now corrected which now checks for the similar type of commands, such as `CMD`, `CMDHELP`, `CMD-HELP`, and `CMD_HELP` and calls the specified function if defined.

**Applies to:** All MCUs

## 8.32 sf\_crypto

**Issue ID:** 12205

When algorithm type is set to MD5, the auto-generated enumerator is now valid. This fix sets the configuration parameter in `sf_crypto_hash` module to a valid enumerator and enables the application project to build successfully.

**Applies to:** S5 and S7 MCU Series

**Issue ID:** 12206

Auto-generated code now uses the ECC domain parameter, as well as the generator point names the user supplies in the Configurator's property settings. The fix impacts backward compatibility and existing projects. When using an SSP version that includes this fix, the user must enter the ECC domain parameter and generator point names that are in use in the Configurator's module properties.

**Applies to:** S5 and S7 MCU Series supporting ECC

**Issue ID:** 12385

The New `KeyInstall2()` API is introduced in the `sf_crypto_key_installation` module. The RSA-wrapped key format that is generated in `sf_crypto_key_installation` module as an output of `keyInstall2` API is the same as the `sf_crypto_key_module/keyGenerate` API. This API is compatible with all other Crypto APIs.

**Applies to:** All S5 and S7 MCU series that support RSA in SCE

**Issue ID:** 12735

When the ECC key size was selected to be 256-bits through the module properties in ISDE at build time, the Domain parameters and Generator Point lengths were set incorrectly in the auto generated code. This in turn would lead to the initialization failure and would not allow any operation with ECC 256-bit key size with that instance.

Now, the auto generated code will set the Domain parameters and Generator Point lengths correctly, allowing the selection of ECC 256-bit keys at build time to successfully generate ECC-256-bit keys.

**Applies to:** S5 and S7 Series of MCUs

## 8.33 sf\_el\_fx

**Issue ID:** 12244

User can access the media information after opening the media with FileX.

**Applies to:** All MCUs with FileX support

**Issue ID:** 11088

The Thread Stack window for FX module turns red and shows the error message "Media size cannot be less than sector size" when the "Working media memory size" value is between 1000 - 5129. To resolve this issue, the "id" for "Working memory Media Size" and the "sector size" in the XML file has been used, and is typecast (by using 'parseInt') for the integer value, which establishes a comparison between them. As a result, the working memory media size greater than sector size is not going to be responsible for any red color pop-up error. Also, the implementation checks that user should not use value less than sector size (if used, it shows an error for the same in the Tool window).

**Applies to:** S7, S5, S3 MCU Series

### 8.34 sf\_el\_gx

**Issue ID:** 9757

The component "GUIX Port on sf\_el\_gx" allows the user to specify the "Display Driver Configuration Inheritance" to "Inherit Graphics Screen 2" (that is, foreground). However, SF\_EL\_GX source always references "DISPLAY\_FRAME\_LAYER\_1" (that is, background) when performing the buffer toggle operation. This configuration is hard-coded in sf\_el\_gx\_frame\_toggle().

The fix introduces a new element inside the "sf\_el\_gx configuration structure" and the instance control structure. It takes the "Display Driver Configuration Inheritance's value" from the user, via the "e2 Studio config tool" and updates the newly created element of the "instance control structure" during sf\_el\_gx initialization; the same is feed while doing buffer toggle operation.

**Applies to:** S7G2 and S5D9 MCU Groups

### 8.35 sf\_el\_nx

**Issue ID:** 10196

Ethernet driver now can detect the MCU and do software padding necessary for S5D5 Mask Rev 02 to fix the ping failure for 4\*N+1 or 4\*N+2 bytes ping length.

**Applies to:** S5D5 MCU Group

**Issue ID:** 11393

The transmitted packets are ensured to have enough space to accommodate all the protocol headers before reaching Ethernet driver.

**Applies to:** S7G2, S5D9, and S5D5 MCU Groups

### 8.36 sf\_el\_tx

**Issue ID:** 11454

Hardware stack monitoring in ThreadX is now supported for all MCUs that have a hardware stack monitor. This issue caused a build error in previous releases for S128 and S1JA MCU Groups.

**Applies to:** S128 and S1JA MCU Groups

### 8.37 sf\_el\_ux

**Issue ID:** 10144

While the USBX Host (all classes) is running on the Synergy board, if the USB device is plugged OFF, then the USBX host application could hang. This behavior only occurred when any thread with any thread priority in application is not suspended (does not have a ThreadX sleep call). This issue is fixed.

**Applies to:** All MCUs boards which support Host class

**Issue ID:** 10577

In some scenarios, a warning message fails to show up in XML configurator for the incorrect Interrupt Priority setting between Transfer modules and USBX controller. This issue is fixed. The comparison of interrupt priority value has to be in such a way that the transfer module interrupt priority must always be higher than the USBX priority.

**Applies to:** All MCUs

**Issue ID:** 10632

Disabling High Speed option field in the configurator for USBX Port HCD on sf\_el\_ux (for USBHS) did not work, and the high-speed operation of the Host controller was not disabled. This issue resulted in no reduction in the power consumption, since the internal PLL of the PHY module and other high-speed analog circuits continue to be clocked. This issue has been fixed.

**Applies to:** S7G2 and S5D9 MCU Groups

**Issue ID:** 11329

The 'ux\_dcd\_synergy\_fifo\_write()' function attempts to set the 'UX\_SYNERGY\_DCD\_FIFOCTR\_BVAL' bit after writing the last packet in a transfer, even if the last packet is the same size as the endpoint buffer size. This resulted in an erroneous generation of Zero length data Packet (ZLP). This logic has been corrected so that an erroneous generation of ZLP is avoided.

**Applies to:** All MCUs

**Issue ID:** 11330

USB DCD - Endpoint reset function is incorrect. This issue limits the reset functionality of the endpoint/pipe as the correct pipe is not properly identified before performing reset, causing an improper reset. This fix identifies the correct pipe to reset and resets it accordingly.

**Applies to:** All MCUs

**Issue ID:** 11407

While using DMA, the USB HS device read was limited to 4K of data. This has been corrected so no limitation exists.

**Applies to:** S5D9 and S7G2 MCU Groups

**Issue ID:** 9482

USBx host MSC project creation using IAR compiler missed a USBFS port pin configuration in the Synergy configuration tool. Once the port pins were configured properly, it worked as usual on IAR as well.

**Applies to:** S3A7 MCU Group

**Issue ID:** 9834

SF\_EL\_UX HCD does not handle the EoF error interrupt in the interrupt handler, even though the interrupt is enabled. Once the EoF error was detected, the driver would be stuck in the interrupt handler; it never cleared the interrupt. The EoF error handling routine is currently not implemented in the driver, but is required since the USB hardware disables the USB port if the error was detected. This issue is fixed in SSP v1.5.0.

**Applies to:** S7G2, S5Dx, and S3Ax MCU Groups

## 8.38 sf\_el\_ux\_comms\_v2

**Issue ID:** 11181

CDC communication framework hung on a ux\_dcd\_synergy\_transfer\_request() function, when the USB cable was unplugged from the HOST PC and re-connected while Tera Term was in a disconnected state. Applicable on Windows 10 PCs only. This issue is fixed.

**Applies to:** S124 MCU Group only

**Issue ID:** 11345

Mutex synchronization errors may occur during lock() and unlock() for sf\_el\_ux\_comms\_v2 when called with SF\_COMMS\_LOCK\_ALL, if the operation succeeds for transmit and fails for receive. This issue is fixed with an error return message SSP\_ERR\_TIMEOUT for unsuccessful lock and SSP\_ERR\_INTERNAL for unsuccessful unlock call.

**Applies to:** All MCUs

**Issue ID:** 11800

Write and read operations in sf\_el\_ux\_comms\_v2 were not thread safe. This issue is fixed using mutexes in read and write APIs.

**Applies to:** All MCUs

**Issue ID:** 12334

When user selects the new stack in the XML configuration for sf\_el\_ux\_comms\_v2, it displayed the name as "communication framework on sf\_el\_ux\_comms". In this release the name has changed to "Communication framework on sf\_el\_ux\_comms\_v2".

**Applies to:** All MCUs

**Issue ID:** 8216

SF\_EL\_UX\_COMMS\_V2 Open function would cause a timeout if the USB CDC-ACM enumeration completes earlier than the semaphore UX\_COMMS\_SEMAPHORE was created in the Open function. In this case, the semaphore is never signaled in the USBX CDC instance\_activate callback function, and Open function continues to suspend until timeout occurred. This issue is fixed.

**Applies to:** All MCUs

### 8.39 sf\_external\_irq

**Issue ID:** 8287

When using the External IRQ Framework, the ISDE allowed the user to change the callback field in the lower level HAL Driver properties. The callback property is now 'locked' and the user cannot change the callback in the lower level driver properties.

**Applies to:** All MCUs

### 8.40 sf\_i2c

**Issue ID:** 10258

I<sup>2</sup>C framework was allowing the opening of same device multiple times. This issue is fixed. Now, I<sup>2</sup>C framework open API returns SSP\_ERR\_ALREADY\_OPEN if same device is opened twice.

**Applies to:** All MCUs

**Issue ID:** 10261

The close API in sci\_i2c was failing after unsuccessful read/write operations because the remaining bytes were not getting reset. The issue is resolved.

**Applies to:** All MCUs

**Issue ID:** 11388

The SF\_I2C module is now supported on S5D9-PK, S3A1-ADK and TB-S1JA boards.

**Applies to:** S5D9, S3A1, and S1JA MCU Groups

**Issue ID:** 11561

Though the I<sup>2</sup>C Framework configurator displays an option to select the slave option; it is not supported by the framework. This fix modifies the xml file to remove the riic\_slave option in the configurator, so it does not display an option to select the riic\_slave.

**Applies to:** All MCUs

### 8.41 sf\_jpeg\_decode

**Issue ID:** 10312

The sf\_jpeg\_decode module closes the low-level driver when the ThreadX API call fails in the sf\_jpeg\_initialize function.

**Applies to:** All supported MCUs

### 8.42 sf\_spi

**Issue ID:** 11087

SPI Framework returns an error code of SSP\_ERR\_TIMEOUT when timeout occurred during read or write operation.

**Applies to:** All supported MCUs

### 8.43 sf\_thread\_monitor

**Issue ID:** 10856

A new configuration property added to the XML for SF\_THREAD\_MONITOR selects the internal thread stack size with default value of 512 bytes.

**Applies to:** All supported MCUs

**Issue ID:** 9435

In the SF\_THREAD\_MONITOR\_Open() API, if the thread create failed, it returned SSP\_SUCCESS. This issue is fixed.

**Applies to:** All MCUs

## 8.44 sf\_touch\_panel\_i2c

**Issue ID:** 11671

The touch driver may provide wrong coordinate information to the application thread, so that the wrong GUIX event can be triggered. This issue was due to a non-optimum configuration setting of the RPNDT value in the SX8654 driver code. This issue was resolved by updating the usage note and refactoring of code so it is easy for the user to change RPNDT setting.

**Applies to:** S7G2 MCU Group

## 8.45 sf\_uart\_comms

**Issue ID:** 11301

The return code of unsuccessful unlock call is changed from SSP\_ERR\_TIMEOUT to SSP\_ERR\_INTERNAL.

**Applies to:** All MCUs

## 8.46 sf\_WiFi

**Issue ID:** 11136

A fix in WiFi NSAL removes the Ethernet header, whether the packet transmission fails or succeeds. Now, when NetX tries to re-transmit a TCP packet, it does not cause an illegal instruction exception.

**Applies to:** WiFi Framework for GT202 on S7G2, S3A7, S5D9, S5D5, S3A6 (only socket), and S3A3 MCU Groups

**Issue ID:** 11337

If enough space is not reserved for all protocol headers in NetX packet, then the WiFi NSAL code drops the packet and does not cause any memory corruption or application malfunction.

**Applies to:** WiFi Framework for GT202 on S7G2, S3A7, S5D9, S5D5, and S3A3 MCU Groups

## 8.47 SSP XMLs for ISDE

**Issue ID:** 10634

If the ARP cache is disabled, no memory is allocated to the cache.

**Applies to:** S7G2, S5D9, S5D5 MCU Groups

**Issue ID:** 11579

S1JA MCU errors are incorrectly reported in e<sup>2</sup> studio if ICLK is configured to be greater than 32 MHz. The maximum ICLK for S1JA is 48 MHz. e<sup>2</sup> studio incorrectly displays an error for the correct ICLK values. The configurator sets the correct ICLK value, but e<sup>2</sup> studio incorrectly reports it on the S1JA, if ICLK is configured to be greater than 32 MHz. This issue has been fixed by checking the upper bounds on ICLK to be 48 MHz on S1JA.

**Applies to:** S1JA MCU Group

**Issue ID:** 12002

Fixed the addresses of several ETHERC registers in the IO register view for S5D5. The affected registers are PTRSTR, SYMACRU, SYMACRL, FFLTR, FMAC0RU, FMAC1RU, FAMC0RL, and FMAC1RL.

**Applies to:** S5D5 MCU Group

## 8.48 USBX

**Issue ID:** 8076

Previously, USBX Device class CDC-ACM enumeration failed on Windows 10 PC (host PC) if the class code property is set to CDC (0x02) in Synergy Configuration tool. This issue is now fixed.

**Applies to:** All MCUs

**Issue ID:** 9166

SF\_EL\_UX - DCD (USBX Port - Device Controller Driver) did not previously support Transaction Abort. Transaction Abort is supported in this release.

**Applies to:** All MCUs

**Issue ID:** 9745

The pre-built library for the USBX Device Class CDC-ACM might not complete data reception if the data is sent from a Host with exactly 64 bytes in case of a Full-Speed connection. A wait for the next byte(s) is needed to determine that the data transfer is complete. This issue is now resolved.

**Applies to:** All MCUs

**8.49 Documentation — IAR Dlib support****Issue ID:** 11045

ThreadX Usage Guide is updated to indicate limitations of Dlib support and additional IAR information on user code that needs to be created to use Dlib features.

**Applies to:** All MCUs

## 9. Known issues and limitations identified in SSP v1.5.0

### 9.1 BSP for SSP supported Platforms

**Issue ID:** 12738

The size of flash memory is incorrect for the S3A6 when using IAR. The linker script has an end address that is past the end of flash.

**Applies to:** S3A6 MCU Group

**Workaround:** Change the linker script to correct the end of flash. Define symbol `region_FLASH_end = 0x0003FFFF`.

**Issue ID:** 11872

When `bsp_api.h` is included in files in Synergy projects, `bsp_common.h` is included before `bsp_cfg.h`. `bsp_common.h` relies on configurations from `bsp_cfg.h`, and these are undefined when `bsp_common.h` is included. As a result, the following macros (that rely on `BSP_CFG_*` macros) are not properly configured:

`SF_CONTEXT_SAVE`

`SF_CONTEXT_RESTORE`

`SSP_ASSERT_FAIL`

`SSP_ERROR_LOG`

`SSP_ASSERT`

`SSP_CRITICAL_SECTION_ENTER`

`SSP_CRITICAL_SECTION_EXIT`

**Applies to:** All MCUs

**Workaround:** Define any macros not set to the default value on the command line.

**Issue ID:** 10664

If a user uses the Trace Buffer for debugging, **and** has data stored in RAM at addresses above `0x2000 4000`, that data is overwritten by the Trace Buffer when debugging.

**Applies to:** S128, S1JA MCU Groups

**Workaround:** The S128 and S1JA linker script currently allocates 1K for the Trace Buffer at `0x2000 0000`. This allocation could be removed, freeing the 1K incorrectly reserved for the Trace Buffer. The e<sup>2</sup> studio Trace Buffer function stores 1K of trace buffer data, beginning at `0x2000 4000`, so 1K of RAM must not be used by the application if the Trace Buffer is used for debugging.

### 9.2 CTSU Development

**Issue ID:** 8731

In the event of a hardware issue where the channel capacitance has an invalid value (due to the board layout), the Capacitive Touch Sensing Unit (CTSU) fails in data acquisition. The code remains in a loop waiting for the data and does not return.

**Applies to:** All MCUs

**Workaround:** Make sure the TSCAP port has the recommended capacitor connected.

### 9.3 Express Logic X-Ware

**Issue ID:** 12908

A multiple symbol definition error may occur during linkage if an X-Ware library component and the corresponding source component such as `ux` and `ux_src` are included. If this occurs, remove the library such as `libux.a` from the list of libraries used by the linker as follows:

- For GCC, in the Cross ARM C Linker > Libraries section of the C/C++ Build > Settings in the project Properties.
- For IAR, in the IAR Linker for ARM > Library section of the C/C++ Build > Settings in the project Properties.

The affected modules are as follows:

- `ux` (USBX)
- `tx` (ThreadX)
- `nx` (NetX)
- `nxd` (NetX Duo)



- fx (FileX)
- gx (GUIX)
- ux\_host\_class\_XXX (USBX Host Classes)
- ux\_device\_class\_XXX (USBX Device Classes).

**Applies to:** All supported Synergy MCU Groups

## 9.4 NetX

**Issue ID:** 11863

The **use server address type** property was default to **IPv6**. It is now changed to **IPv4** address type.

**Applies to:** S7G2, S5D9, S5D5 MCU Groups

**Workaround:** None

**Issue ID:** 12294

On fetching volume entry label from some USB storage drives, FTP server can get negative index for month value, which results in hard fault (for invalid address) or stack corruption.

**Applies to:** S7G2, S5D9, S5D5 MCU Groups

**Workaround:** None

**Issue ID:** 12951

Users will not be able to use TLS 1.0 for secure connection.

**Applies to:** S7G2, S5D9, S5D5, S5D3 MCU Groups

## 9.5 nxd\_mqtt\_client

**Issue ID:** 13048

MQTT client, `nxd_mqtt_client_secure_connect()`, invokes `tls_setup()` but never checks for its return value. Even when `tls_setup()` returns error, `nxd_mqtt_client_secure_connect()` continues to execute, which is not desired.

**Applies to:** S7G2, S5D9 MCU Groups

**Workaround:** None

**Issue ID:** 10751

The application may hang if it tries to subscribe (using `nxd_mqtt_client_subscribe()`) to MQTT topic in quick succession.

For example, the application may hang if it tries to publish messages (using `nxd_mqtt_client_publish()`) to topic in quick succession followed by attempt to read back (using `nxd_mqtt_client_message_get()`) the message from broker, for example, publishing 1000 messages.

**Applies to:** S7G2 and S5D9 MCU Groups

**Workaround:** Application should avoid reading back messages from broker after doing MQTT publish to a topic in quick succession

**Issue ID:** 12395

The API `nxd_http_client_put_start()` is used to start a PUT operation. It takes as input username/password. There is an issue when an application is built using optimization `-O2` and passes username/password as NULL to `nxd_http_client_put_start()` API. The issue is that, due to optimization, NULL username/password are treated as non-NULL.

**Applies to:** S5D9 and S7G2 MCU Groups

**Workaround:** Use optimization level 0(`-O0`) if permissible.

**Issue ID:** 12357

When MQTT client application uses `nxd_mqtt_client_client_login_set()` API and passes null username to API, the username/password credentials are not passed to MQTT server. As a result, MQTT client cannot connect to MQTT server.

**Applies to:** S5D9 and S7G2 MCU Groups

**Workaround:** None

## 9.6 nxd\_tls\_secure

**Issue ID:** 12940

Applications requiring TLS connection will not be functional when connecting with servers strictly enforcing section 3.4 of RFC 5746.

**Applies to:** S5 and S7 MCU Series

**Workaround:** Contact Technical Support/Sales FAE for more information.

**Issue ID:** 13044

Using NetX Secure in C++ applications results in compiler error.

**Applies to:** All MCUs

**Workaround:** None

## 9.7 r\_agt

**Issue ID:** 12684

The periodSet API sets an incorrect time period, when clock source is PCLKB and period is changed from a higher value to a lower value. (for example, when period is changed from 10 ms to 1 ms when PCLKB is 24 MHz)

**Applies to:** All MCUs

**Workaround:** Close and re-open the driver before changing the period from a higher value to lower value.

## 9.8 r\_can

**Issue ID:** 12432

Once an error condition is reported in ECSR, it will always be reported by statusGet because the ECSR is never cleared.

**Applies to:** All MCUs

**Workaround:** Clear the ECSR manually after calling statusGet.

## 9.9 r\_cgc

**Issue ID:** 12322

When PLL clock is active, PLLSTP = 0, but is not the current system clock, then if the user tries to stop the source clock to PLL (it can be either MOCO or main-clock), the clock stop API returns success, but the source clock doesn't stop as indicated by MOSTP = 0 or MCSTP = 0, as it is supplying clock to PLL.

**Applies to:** All MCU Series except S1

**Workaround:** Stop the PLL clock, and then stop the source clock to PLL (MOCO or main-clock).

## 9.10 r\_dac8

**Issue ID:** 12261

DAC8 output pin is not getting configured when it is configured through ISDE.

**Applies to:** S1JA, S128, and S3A3 MCU Groups

**Workaround:** Configure DAC8 output pin manually.

## 9.11 r\_flash\_hp

**Issue ID:** 7578

If FCLK is set to a frequency less than the maximum FCLK setting of 60 MHz, then the FACL command processing does not run at the optimum rate and incurs additional unnecessary processing overhead.

As a result, the performance of Flash operations such as overwriting will take longer than the optimal duration.

**Applies to:** All MCUs

**Workaround:** None

## 9.12 r\_flash\_lp, r\_flash\_hp

**Issue ID:** 12435

If code running from SRAMHS (0x1FFE 0000 - 0x1FFF FFFF) tries to program the option setting memory, then the option setting memory may be corrupted. This may cause the flash access window to be set or an unknown ID code to be set.

**Applies to:** S5D3, S5D5, S5D9 MCU Groups

**Workaround:** Ensure that any code that programs the option setting memory is located in SRAM0 (0x2000 0000 - 0x2003 FFFF).

## 9.13 r\_gpt

**Issue ID:** 12676

In GPT one shot mode, after opening the GPT driver, GPT start() is called and one pulse is generated at GPT output pin. When GPT start() is called again, no further pulses are generated unless the GPT driver is closed and reopened.

**Applies to:** All MCUs

**Workaround:** User should close and reopen the driver each time before calling gpt\_start() API

## 9.14 r\_jpeg\_encode

**Issue ID:** 12511

After encoding the last chunk of image, the driver must invoke callback with done status. But the driver invokes callback with input\_pause status first, and then invokes callback with done status.

**Applies to:** S7G2, S5D9 MCU Groups

**Workaround:** Check the number of lines provided to the driver and ignore the callback with extra input\_pause status invoked after encoding the last chunk of data.

## 9.15 r\_qspi

**Issue ID:** 12917

Quad input page program and dual input page program only worked if the p\_spi\_mode parameter from bsp\_qspi\_config\_get is set incorrectly (set to quad/dual mode even though the device is in extended SPI mode).

**Applies to:** S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2 MCU Groups

**Workaround:** None

## 9.16 r\_riic

**Issue ID:** 13047

The open R\_RIIC\_MasterOpen API configures the DTC for both receive and transmit operations. However, the driver function which configures the DTC does not return the actual status. Return variable of the function is always overwritten with the subsequent condition checks and a failure in the initial checks is never returned.

**Applies to:** All MCUs

**Workaround:** None

**Issue ID:** 11562

RIIC\_Slave read operation provides the wrong count on number of bytes received. This wrong information is provided in the callback if number of bytes received from the master are less than the expected number of bytes at the Slave.

**Applies to:** All MCUs

**Workaround:** None

## 9.17 r\_rsipi

**Issue ID:** 11592

When using DTC, the following is observed:

- SPI\_EVENT\_ERR\_MODE\_UNDERRUN error occurs for 1-byte width transfer for clock rates greater than 5MHz
- The code goes to the default\_handler while using 2-byte and 4-byte data widths, for all clock rates.

**Applies to:** S5D9 MCU Group

**Workaround:** Use CPU copy and interrupts instead of DTC

## 9.18 r\_sci\_uart

**Issue ID:** 12502

In R\_SCI\_UART driver, if user selects non-fifo sci channel and writing data to TDRE register due to interrupt race condition, user gets an error return of SSP\_ERR\_IN\_USE.

**Applies to:** S1 MCU Series, S3A6 and S3A3 MCU Groups

**Workaround:** Close and open the driver, and perform write operation.

**Issue ID:** 11268

Some of the received bytes may get corrupted/missed due to errors during reception when the DTC is used for reception with data length greater than 1KB.

**Applies to:** All MCUs

**Workaround:** Do not add a DTC for RX in the UART configurator, instead use callback function to get the data.

## 9.19 r\_sdmmc

**Issue ID:** 13056

eMMC cards that take longer than one second to de-assert the busy signal after CMD6 may not work with the r\_sdmmc driver.

**Applies to:** S7G2, S5D9, S5D5, S5D3, S3A7, S3A3, S3A1 MCU Groups

**Workaround:** Add a delay after open() until the DAT0 line is cleared before using other r\_sdmmc APIs.

## 9.20 sf\_adc\_periodic

**Issue ID:** 13033

ThreadX resources initialized in open API are not released if an error is returned. This causes failure of subsequent open calls in the framework.

**Applies to:** All MCUs

**Workaround:** None

## 9.21 sf\_block\_media\_lx\_nor

**Issue ID:** 12861

Direct read from flash is not supported.

**Applies to:** All MCUs/boards supporting LevelX NOR

**Workaround:** None

## 9.22 sf\_block\_media\_qspi

**Issue ID:** 12855

If an error occurs during a lower-level read or write call, the read()/write() API returns without returning the mutex.

**Applies to:** All MCUs

**Workaround:** If the error occurs in read() or write() for sf\_block\_media\_qspi, close and reopen the module before using the module from another thread.

## 9.23 sf\_cellular

**Issue ID:** 12844

sf\_cellular\_cat1\_connect API returns success even though the connection is not established.

**Applies to:** NimbeLink CAT1 module

**Workaround:** None

**Issue ID:** 12950

Reconnecting to the cellular network fails after disconnecting from the network using Cellular Framework Disconnect API.

**Applies to:** Cellular framework for Quectel CATM1 on NB-IoT

**Workaround:** User will have to delete the NetX IP and PPP instances using nx\_ip\_delete() and nx\_ppp\_delete() APIs respectively, and then recreate the IP instance using nx\_ip\_create().

**Issue ID:** 11846

While downloading large size data, packets are received at NETX socket level but getting those packets using netx protocols such as http, ftp, and so forth, fails which results in Download failure in case of CAT3 TSVG Modem. This issue is not observed with the CAT3 TEUG modem.

**Applies to:** Cellular Framework for NimbeLink CAT3 TSVG modules on Verizon Network

**Workaround:** None

**Issue ID:** 12355

`nx_ip_delete()` when invoked, is responsible for releasing all system resources related to WiFi/Cellular Framework. However, invocation of `nx_ip_delete()` does not release system resources related to WiFi/Cellular Framework.

**Applies to:** WiFi and Cellular Framework

**Workaround:** User should invoke `nx_ip_delete()` followed by `close()` to release all system resources for WiFi/Cellular Framework in order to completely shut it down.

**Issue ID:** 12257

PPP link goes down when running the Cellular Application with NetX Duo.

**Applies to:** NimbeLink CAT1 on all Synergy MCUs.

**Workaround:** The Application can restart NetX PPP instance using `nx_ppp_restart()` from PPP Link down notification callback handler that it has registered with the framework.

**Issue ID:** 12266

While downloading large size data, packets are received at NetX socket level but getting those packets using netx protocols such as http, ftp, and so forth fails, which results in download failure in case of NimbeLink CAT1 Modem.

**Applies to:** Cellular Framework for NimbeLink CAT1 modules on Verizon Network

**Workaround:** None

## 9.24 sf\_console

**Issue ID:** 12918

The function `sf_console_prompt` returns `SSP_SUCCESS` even if an unsupported command is passed to the console. If the user enters an invalid command, it should return `SSP_ERR_UNSUPPORTED`.

**Applies to:** All MCUs

**Workaround:** None

## 9.25 sf\_crypto

**Issue ID:** 12796

`SSP_ERR_INVALID_SIZE` and `SSP_ERR_INVALID_ARGUMENT` are listed as a return values for `keyInstall` API and `keyInstall2` APIs. `SSP_ERR_INVALID_ARGUMENT` is returned when an incorrect buffer size is passed instead of `SSP_ERR_INVALID_SIZE`.

However, `keyInstall2` API returns the correct error code for RSA key type.

**Applies to:** S3, S5 and S7 MCU series

**Workaround:** None/not applicable

## 9.26 sf\_crypto/Synergy Tools

**Issue ID:** 12724

Build fails after changing the device in the project with crypto module that was already built with IAR toolchain. This is because the project still refers to the old crypto library that was deleted when the device is changed and project is regenerated.

**Applies to:** All MCUs

**Workaround:** Right click the project and select properties. Go to the setting page under C/C++ build and delete the old library from the library page under IAR Linker for ARM and regenerate the project.

## 9.27 sf\_el\_fx

**Issue ID:** 12793

Synergy generated code for FileX will not check if the file system has been initialized for the media or not. Due to this, FileX will format the media after every power cycle or reset, if **Format during initialization** option is enabled.

**Applies to:** All Supported MCUs

**Workaround:** Disable the **Auto Initialization** option from the FileX configuration property User needs to follow these steps in their application to avoid media formatting during power cycle or reset: Open the `fx_media` and check for the error. If the errors are `FX_BOOT_ERROR`, `FX_MEDIA_INVALID` and `FX_FAT_READ_ERROR`, then format the media and open the `fx_media` again.

## 9.28 sf\_el\_gx

**Issue ID:** 12760

Applications using the GUIX will give build error if built with C++ compiler. The `gx_display.h` file in `synergy/ssp/inc/framework/el` does not include `SSP_HEADER` and `SSP_FOOTER` macro. These macros wrap contents in extern "C" when C++ compiler is used. This file is then included through `sf_el_gx_api.h`, which is included from GUIX Studio-generated code for Synergy targets. As these macros are missing from `gx_display.h`, build error will occur if GUIX applications are compiled with C++ compiler.

**Applies to:** S7G2 and S5D9 MCU Groups

**Workaround:** The build error can be avoided by moving the `#include "gx_display.h"` immediately after `SSP_HEADER` in `sf_el_gx_api.h`.

**Issue ID:** 13030

The GUIX shapes such as circle, arc, polygon, eclipse, pie, and text (1bpp and 4bpp) will not be rendered properly if D/AVE 2D accelerator is enabled in the application. This happens because of the incorrect configuration of the D/AVE 2D accelerator while rendering these GUIX shapes.

**Applies to:** S7G2 and S5D9 MCU Groups

**Workaround:** Disable D/AVE 2D accelerator when the above specified GUIX shapes are used in the application.

## 9.29 sf\_el\_tx

**Issue ID:** 10703

TraceX time measurement does not work out-of-the box for CM0+ parts.

**Applies to:** S124 and S128 MCU Groups

**Workaround:** Define `TX_TRACE_TIME_SOURCE` on the command line to the SysTick address (0xE000E018).

**Issue ID:** 12423

The stack monitor will not detect an underflow of one word at the end of the main stack. In the unlikely event that the stack underflowed, one word beyond the end of the stack can be overwritten.

**Applies to:** S7G2, S5D9, S5D5, S5D3, S3A7, S3A6, S3A3, S3A1, S128, S1JA

**Workaround:** None

## 9.30 sf\_el\_ux

**Issue ID:** 12758

In the USBHS peripheral, the USBMCLK (20 or 24 MHz) is supplied from the Main oscillator clock for the functioning of USBHS peripheral in non-CL only mode. The USBHS is not functional with the clock setting in the Synergy configurator set to any unsupported value. This is expected behavior for unsupported clock value. However, there is no warning message displayed in the synergy clock tree configurator when the Main oscillator clock is wrongly configured.

**Applies to:** S7G2 and S5D9 MCUs

**Workaround:** User should explicitly configure the Main oscillator clock in the clock tree of the Synergy configurator. User should configure as specified in the MCU hardware user's manual.

**Issue ID:** 10575

USBX device class does not support the remote wake up feature.

**Applies to:** All MCUs

**Workaround:** None

**Issue ID:** 11332

SF\_EL\_UX Device driver is not functional when DTC is configured as the transfer component in the Synergy configuration tool to the USBX Device Class stack.

This issue is applicable only for USB device classes.

**Applies to:** All MCUs

**Workaround:** Instead of using DTC as a transfer component to the USBx Device class stack, use DMA or CPU (software) as the transfer component in the Synergy configuration tool. On S1 parts, since DMA is not supported, use CPU (software) as the transfer component.

### 9.31 sf\_el\_ux\_comms\_v2

**Issue ID:** 11533

In the sf\_el\_ux\_comms\_v2 module, the Open API creates a semaphore, but does not release the semaphore when Close API is called.

**Applies to:** All MCUs

**Workaround:** The user application should delete the semaphore which was created in the Open API. For example, insert the following in application code to delete the semaphore:

```
err = tx_semaphore_delete(&g_sf_comms0_instance_ctrl.semaphore);  
ssp_err = g_sf_console0.p_api->close(g_sf_console0.p_ctrl);
```

### 9.32 sf\_i2c

**Issue ID:** 12414

If any I<sup>2</sup>C Framework device calls close() API, it will close the low level driver. Once the low level driver is closed, any attempt from other I<sup>2</sup>C framework devices to perform read/write operations on the bus will fail. The other devices will not be able to open the lower device in this case if device count is not zero. Hence, further operations on shared I<sup>2</sup>C bus will be unsuccessful.

**Applies to:** All MCUs

**Workaround:** The user application should not call close() API unless all other devices finish their read/write operations.

### 9.33 sf\_spi

**Issue ID:** 13017

When SF\_SPI is used with RSPI at low-level and DTC, the read/write call sometimes fails when writing 1 Mb of data.

**Applies to:** S128 MCU Group

**Workaround:** None

### 9.34 sf\_uart\_comms

**Issue ID:** 12851

If creation of required RTOS objects fails in open(), the module cannot be reopened unless the control block memory is cleared.

**Applies to:** All MCUs

**Workaround:** Clear the control block memory (<sf\_uart\_comms0>.p\_ctrl) before reopening sf\_uart\_comms after open fails.

**Issue ID:** 12995

The SF\_UART\_COMMS read() API does not return an error if the internal read queue overflows; instead, it silently discards the received data. This happens if the read queue size is configured to a lesser value in the SF\_UART\_COMMS configurator.

**Applies to:** All MCUs

**Workaround:** Increase the read queue size in the SF\_UART\_COMMS configurator property.

### 9.35 sf\_WiFi

**Issue ID:** 11044

Receiving and transmitting UDP packets at high throughput through the WiFi module can cause connection failure.

**Applies to:** GT202 WiFi Framework for GT202 on S7G2, S3A7, S5D9, S5D5, S3A6 (only socket), and S3A3 MCU Groups

**Workaround:** None

## 9.36 Synergy Tools

**Issue ID:** 12356

Support for ID byte programming for S128 devices is not available in SEGGER J-Link DLL version 6.32.

**Applies to:** S128 MCU Group

**Workaround:** None

## 9.37 Tx

**Issue ID:** 12909

Enabling "No Timer" option in ThreadX source code results in compilation error.

**Applies to:** All MCUs

**Workaround:** None

## 9.38 USBX

**Issue ID:** 12075

When the Synergy board is configured to work as any supported USBx Host class, there is a possibility that transfer descriptor variable (`hcd_synergy > ux_hcd_synergy_number_tds`) rolls over as this variable is incremented continuously in `sf_el_ux` driver, causing undesirable behavior.

**Applies to:** All Synergy MCUs

**Workaround:** None

**Issue ID:** 12531

When a Synergy board is configured as a USB device Mass storage class, user will not be able to change the USB MSC device storage vendor id as this is hard coded to "ExpressL".

**Issue ID:** 6470

Module name: `ux_host_class_prolific` (USBX Host Prolific Class)

USBX Host Class Prolific is currently included in the SSP package as an experimental, untested module; its functionality is not guaranteed.

**Workaround:** Not applicable

**Issue ID:** 11293

When MSC and CDC composite classes are used in the same project, if the CDC class does not respond, the MSC class also fails to get the MSC device content.

**Applies to:** All MCUs

**Workaround:** None

**Issue ID:** 11508

USB Device MSC with DMA on S3A1 cannot copy large files (that is, more than 20 KB files) from host (PC) to device (Synergy board).

**Applies to:** S3A1 MCU Group

**Workaround:** To copy large files, use CPU mode instead DMA mode in synergy configuration tool.



## 10. Complete list of modules available in this release

These modules are available for respective MCUs based on the following criteria:

- If the core functionality of the module has been tested and works on a MCU, even if it has known bugs, then the module is supported on the MCU.
- If the core functionality is broken or not tested on a MCU then that module is not supported on the MCU.
- If a module has been tested on one of the Synergy MCUs, and it is independent of the underlying MCU hardware or HAL drivers, then the module is supported on all Synergy MCUs on which the underlying driver/framework/stack upon which the module depends on have been completely tested on that MCU.

### 10.1 BSP and Driver Modules available in this release

Module Name	SSP Feature	Supported Synergy MCU Groups
BSP	Board Support Package	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D5, S5D9, S7G2, S5D3
<b>Driver</b>		
r_acmphs	Analog Comparator High Speed	S1JA
r_acmplp	Analog Comparator Low Power	S1JA
r_adc	A/D Converter	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_agt	Asynchronous General Purpose Timer	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_cac	Clock Frequency Accuracy Measurement Circuit	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_can	Controller Area Network	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_cgc	Clock Generation Circuit	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_crc	Cyclic Redundancy Check Calculator	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_cts	Capacitive Touch Sensing Unit	S124, S128, S3A7, S5D5, S5D9, S7G2
r_dac	Digital to Analog Converter	S124, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_dac8	8-bit Digital to Analog Converter	S128, S1JA, S3A3
r_dmac	Direct Memory Access Controller	S3A1, S3A3, S3A6, S3A7, S5D5, S5D3, S5D9, S7G2
r_doc	Data Operation Circuit	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_dtc	Data Transfer Controller	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_elc	Event Link Controller	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_flash_hp	Flash Memory, High Performance	S5D3, S5D5, S5D9, S7G2
r_flash_lp	Flash Memory, Low Power	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7
r_fmi	Factory Microcontroller Information	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_glcd	Graphics LCD Controller	S5D9, S7G2
r_gpt	General Purpose Timer	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_gpt_input_capture	General Input Capture	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_icu	Interrupt Controller Unit	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_ioport	General Purpose I/O Ports	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2

r_iwdt	Independent Watchdog Timer	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_jpeg_common	JPEG Common	S5D9, S7G2
r_jpeg_decode	JPEG Decode	S5D9, S7G2
r_jpeg_encode	JPEG Encode	S5D9, S7G2
r_kint	Keyboard Interrupt Interface	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_lpm†	Low Power Mode	S124, S3A7, S7G2
r_lpmv2_s1ja	Low Power Mode V2 for S1JA	S1JA
r_lpmv2_s124	Low Power Mode V2 for S124	S124
r_lpmv2_s128	Low Power Mode V2 for S128	S128
r_lpmv2_s3a1	Low Power Mode V2 for S3A1	S3A1
r_lpmv2_s3a3	Low Power Mode V2 for S3A3	S3A3
r_lpmv2_s3a6	Low Power Mode V2 for S3A6	S3A6
r_lpmv2_s3a7	Low Power Mode V2 for S3A7	S3A7
r_lpmv2_s5d3	Low Power Mode V2 for S5D3	S5D3
r_lpmv2_s5d5	Low Power Mode V2 for S5D5	S5D5
r_lpmv2_s5d9	Low Power Mode V2 for S5D9	S5D9
r_lpmv2_s7g2	Low Power Mode V2 for S7G2	S7G2
r_lvd	Low Voltage Detection Driver	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_opamp	Operational Amplifier	S1JA
r_pdc	Parallel Data Capture Unit	S5D5, S7G2
r_qsapi	Quad Serial Peripheral Interface	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
r_riic	IIC	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_riic_slave	IIC Slave	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_rsapi	Serial Peripheral Interface	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_rtc	Real-time Clock	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_sci_i2c	Serial Communication Interface I2C	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_sci_spi	Serial Communication Interface SPI	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_sci_uart	Serial Communication Interface UART	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_sdadc	Sigma Delta ADC	S1JA
r_sdmmc	SDHI Driver for SDIO and SD/MMC Memory Devices	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
r_slcdc	Segment LCD Controller	S3A1, S3A3, S3A6, S3A7
r_ssi	(Inter-IC Sound) Interface [old: Serial Sound Interface] or r_i2s	S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_wdt	Watchdog Timer	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_sce#	Cryptographic Library (HAL interfaces)	See table note on Cryptographic Functions.

# **Cryptographic Functions:** Section 10.4 lists cryptographic functions available for each MCU in this release; these functions are accessible as part of r\_sce/cryptographic library.

## 10.2 Framework Modules available in this release

Module Name	SSP Feature	Supported Synergy MCU Groups
sf_adc_periodic	Periodic Sampling ADC	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_audio_playback	Audio Playback	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_audio_playback_hw_dac	Audio Playback HW DAC	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_audio_playback_hw_i2s	Audio Playback HW I2S	S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_audio_record_adc	Audio Record ADC	S124, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_audio_record_i2s	Audio Record I2S	S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_ble_rl78g1d	BLE Framework	S128, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2, S3A1, S124
sf_ble_rl78g1d_onboard_profile	BLE Framework Onboard Profiles	S124, S128, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2, S3A1
sf_block_media_lx_nor	Block Media Interface for LevelX NOR	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
sf_block_media_qspi	Block Media Interface for QSPI	S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
sf_block_media_ram	Block Media Interface for RAM	S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_block_media_sdmmc	Block Media Interface for SD Multi Media Card	S3A3, S3A7, S5D3, S5D9, S7G2, S3A1, S5D5
sf_comms_telnet	Telnet Communications	S5D3, S5D5, S5D9, S7G2
sf_console	Console	S124, S128, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_el_fx	Synergy FileX interface	S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_el_gx	Synergy GUIX Interface	S7G2, S5D9
sf_el_lx_nor	Synergy LevelX NOR Interface	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
sf_el_nx	Synergy NetX Interface	S5D5, S5D9, S7G2
sf_el_nx_comms	Synergy NetX Communication Interface	S5D5, S5D9, S7G2
sf_el_ux	Synergy USBX Interface	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D5, S5D9, S5D3, S7G2
sf_el_ux_comms†	Synergy USBX Communication Interface	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D5, S5D9, S7G2
sf_el_ux_comms_v2	Synergy USBX Communication Interface V2	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D5, S5D9, S5D3, S7G2
sf_external_irq	External Interrupt	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_i2c	I2C Framework	S124, S128, S3A3, S3A6, S3A7, S5D3, S5D5, S7G2
sf_jpeg_decode	JPEG Decode	S5D9, S7G2
sf_memory_qspi_nor	Memory QSPI NOR	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
sf_message	Inter-Thread Messaging	S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_power_profiles†	Power Mode Profile	S124, S3A7, S7G2
sf_power_profiles_v2	Power Mode Profile V2	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_spi	SPI Framework	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2

sf_tes_2d_drw	2D Drawing Engine Framework	S5D9, S7G2
sf_thread_monitor	Thread Monitor (Watchdog)	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_touch_ctsu	Capacitive Touch Sensing Unit	S124, S128, S3A3, S3A7, S5D9, S7G2
sf_touch_ctsu_button	Capacitive Touch Sensing Unit Button	S124, S128, S3A3, S3A7, S5D9, S7G2
sf_touch_ctsu_slider	Capacitive Touch Sensing Unit Slider	S124, S128, S3A3, S3A7, S5D9, S7G2
sf_touch_panel_i2c	Touch Panel I <sup>2</sup> C	S5D9, S7G2
sf_touch_panel_v2	Touch Panel Version 2	S5D9, S7G2
sf_uart_comms	UART Framework	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_wifi_gt202	WiFi Framework	S124, S128, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
sf_wifi_gt202_onchip	WiFi framework on Chip Stack	S124 (gcc), S128, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_cellular_catm1	Cellular Framework Quectel BG96 CATM1 & NB-IOT	S5D9, S7G2
sf_cellular_catm1_socket	Cellular Framework Quectel BG96 CATM1 & NB-IOT On Chip Stack	S5D9, S7G2
sf_cellular_cat1	Cellular Framework Nimbelinek CAT1	S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
sf_cellular_cat1_socket	Cellular Framework Nimbelinek CAT1 Socket	S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_cellular_cat3	Cellular Framework Nimbelinek CAT3	S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
sf_cellular_cat3_socket	Cellular Framework Nimbelinek CAT3 Socket	S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_crypto <sup>#</sup> , ##	Cryptographic Framework	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_el_nx_crypto	Cryptographic framework- Shim layer	S7G2, S5D9, S5D5, S5D3

# **Cryptographic Functions:** Section 10.4 lists cryptographic functions available for each MCU in this release; these functions are accessible as part of r\_sce/cryptographic library.

## Framework Interfaces for Cryptographic Functions (sf\_crypto) available for this release include: HASH, TRNG, and Key Generation (RSA and AES).

† Indicates a module that is deprecated starting with SSP v1.3.0 and all subsequent versions. Deprecated modules will only be available to maintain compatibility with existing projects that may be using them. It is highly recommended that new projects use the recommended replacements and not use deprecated modules. For details, see the SSP User's Manual.

### 10.3 Third-Party Modules available in this release

Module Name	SSP Feature	Supported Synergy MCU Groups
fx	FileX	S124, S3A3, S3A6, S3A7, S5D9, S7G2
gx	GUIX	S5D9, S7G2
nx	NetX	S3A7, S3A3, S3A1, S5D3, S5D5, S5D9, S7G2
nx_auto_ip	NetX Auto IP	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nx_bsd	NetX BSD	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nx_dhcp_client	NetX DHCP Client	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nx_dhcp_server	NetX DHCP Server	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nx_dns_client	NetX DNS Client	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nx_ftp_client	NetX FTP Client	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nx_ftp_server	NetX FTP Server	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nx_http_client	NetX HTTP Client	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nx_http_server	NetX HTTP Server	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nx_pop3	NetX POP3	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nx_ppp	NetX PPP	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2*
nx_smtp_client	NetX SMTP Client	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nx_snmp	NetX SNMP Agent	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nx_snmp_client	NetX SNMP Client	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nx_telnet_client	NetX Telnet Client	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nx_telnet_server	NetX Telnet Server	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nx_tftp_client	NetX TFTP Client	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nx_tftp_server	NetX TFTP Server	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
Nxd	NetX Duo Stack	S3A7, S3A3, S3A1, S5D3, S5D5, S5D9, S7G2
nxd_auto_ip	NetX Duo Auto IP	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nxd_bsd	NetX Duo BSD	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nxd_dhcp	NetX Duo DHCP IPv4 Client	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nxd_dhcp	NetX Duo DHCP IPv6 Client	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nxd_dhcp_server	NetX Duo DHCP IPv4 Server	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nxd_dhcp_server	NetX Duo DHCP IPv6 Server	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nxd_dns	NetX Duo DNS Client	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nxd_ftp_client	NetX Duo FTP Client	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nxd_ftp_server	NetX Duo FTP Server	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nxd_http_client	NetX Duo HTTP Client	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nxd_http_server	NetX Duo HTTP Server	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nxd_nat	NetX Duo NAT	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nxd_pop3	NetX Duo POP3	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nxd_ppp	NetX Duo PPP	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2*
nxd_smtp_client	NetX Duo SMTP Client	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nxd_snmp	NetX Duo SNMP Agent	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nxd_snmp_client	NetX Duo SNMP Client	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nxd_telnet_client	NetX Duo Telnet Client	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nxd_telnet_server	NetX Duo Telnet Server	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nxd_tftp_client	NetX Duo TFTP Client	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nxd_tftp_server	NetX Duo TFTP Server	S3A7*, S3A3*, S3A1*, S5D3*, S5D5*, S5D9*, S7G2
nxd_mqtt_client	NetX Duo MQTT Client	S3A7*, S3A3*, S3A1*, S5D3, S5D5, S5D9, S7G2
nxd_tls_secure	NetX Duo TLS Secure	S5D9, S7G2
nxd_web_http_client	NetX Duo Web HTTP1.1 Client	S5D3*, S5D5*, S5D9, S7G2
	NetX Duo Web HTTPS Client	S5D9, S7G2

Tx	ThreadX	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
Lx_nor	LevelX NOR	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
ux_device_class_storage	USBX Device Class Mass Storage	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D9, S7G2, S5D3, S5D5
ux_device_class_hid	USBX Device Class HID	S124, S128, S3A3, S3A6, S3A7, S5D9, S7G2, S5D3, S5D5, S3A1, S1JA
ux_device_class_cdc_acm	USBX Device Class CDC-ACM	S124, S128, S3A3, S3A6, S3A7, S5D9, S7G2, S5D3, S5D5, S3A1, S1JA
ux_host_class_cdc_acm	USBX Host Class CDC-ACM	S3A3, S3A7, S5D9, S7G2, S5D3, S5D5, S3A1
ux_host_class_hid	USBX Host Class HID	S3A3, S3A7, S5D9, S7G2, S5D3, S5D5, S3A1
ux_host_class_hub	USBX Host HUB	S5D9, S7G2, S5D3, S5D5
ux_host_class_storage	USBX Host Class Mass Storage	S3A1, S5D3, S5D5, S3A3, S3A7, S5D9, S7G2
ux_host_class_video	USBX Host Video class	S5D9, S7G2

\* NetX and NetX Duo Applications are MCU-independent application layer protocols dependent on the NetX and Ethernet drivers. All MCUs on which NetX has been tested and verified support these protocols.

### 10.4 Cryptographic functions for each MCU available in this release

Function	S7G2, S5D9, S5D5, S5D3	S3A1, S3A3, S3A7, S3A6	S1JA, S124, S128
TRNG	Generate and read random number	Generate and read random number	Generate and read random number
AES	Encryption, decryption, Key Generation - wrapped keys	Encryption, decryption, Key Generation - wrapped keys	Encryption, decryption
AES Key Size	128-bit, 192-bit, 256-bit	128-bit, 256-bit	128-bit, 256-bit
AES Key Type	Plain text / raw key, Wrapped key	Plain text / raw key, wrapped key	Plain text / raw key
AES Chaining Modes	ECB, CBC, CTR, GCM, XTS <sup>††</sup>	ECB, CBC, CTR, GCM, XTS	ECB, CBC, CTR
ARC4	Encryption, decryption	NA	NA
TDES	Encryption, decryption	NA	NA
TDES Key Size	192-bit	NA	NA
TDES Chaining Modes	ECB, CBC, CTR	NA	NA
RSA	Signature Generation, Signature Verification, Public-key Encryption, Private-key Decryption, Key Generation - plain text and wrapped keys	NA	NA
RSA Key Size	1024-bit, 2048-bit	NA	NA
RSA Key Type	Plain text / raw key, Wrapped key	NA	NA
Key Installation	AES, ECC, RSA keys	AES keys	NA
ECC	Key Generation, Scalar Multiplication, ECDSA – Signature Generation, ECDSA – Signature Verification, (see usage notes for plain text key preparation)	NA	NA
ECC Key Size (in bits)	192, 224, 256, and 384	NA	NA
ECC Key Type	Plain text/ raw keys and wrapped keys	NA	NA

Function	S7G2, S5D9, S5D5, S5D3	S3A1, S3A3, S3A7, S3A6	S1JA, S124, S128
DSA	Signature Generation, Signature Verification	NA	NA
DSA Key Size	(1024, 160)-bit, (2048, 224)-bit, (2048, 256)-bit	NA	NA
HASH	SHA1, SHA224, SHA256, MD5	NA	NA

†† XTS is supported for 128-bit and 256-bit keys only.

## 10.5 Experimental Modules available in this release

**Experimental modules:** Modules that have not been tested on the MCUs, have been classified as experimental modules and are listed in the following table. These experimental modules are currently not supported by Synergy Configuration tools and use of these modules in customer projects is not supported by Renesas at this time.

Experimental Modules		
ux_device_class_cdc_ecm	USBX Device Class CDC-ECM	S124, S3A3, S3A7, S5D9, S7G2
ux_device_class_rndis	USBX Device Class RNDIS	S124, S3A3, S3A7, S5D9, S7G2
ux_host_class_gser	USBX Host Class Generic Serial	S3A3, S3A7, S5D9, S7G2
ux_host_class_printer	USBX Host Class Printer	S3A3, S3A7, S5D9, S7G2
ux_host_class_prolific	USBX Host Class Prolific	S3A3, S3A7, S5D9, S7G2
ux_host_class_swar	USBX Host Class Swar	S3A3, S3A7, S5D9, S7G22
ux_network_driver	USBX Network Driver	S124, S3A3, S3A7, S5D9, S7G2
nxd_web_http_server	NetX Duo Web HTTP Server	S5D9, S7G2

## 11. Additional technical notes

- Subscribe to the Synergy Technical Bulletin Board to receive the latest technical news and notifications about new features, known issues, workarounds, and release announcements. To subscribe, visit [http://renesasrulz.com/synergy/synergy\\_tech\\_notes/f/214.aspx](http://renesasrulz.com/synergy/synergy_tech_notes/f/214.aspx). Sign in to Renesas Rulz, and press **Email Subscribe to this forum**.
- Additional technical information, including informative papers and articles on SSP and Synergy can be found at Synergy Knowledge Base: [www.renesassynergy.com/knowledgebase](http://www.renesassynergy.com/knowledgebase)



## Website and Support

Visit the following vanity URLs to learn about key elements of the Synergy Platform, download components and related documentation, and get support.

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Software glossary	<a href="https://renesassynergy.com/softwareglossary">renesassynergy.com/softwareglossary</a>
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MCU glossary	<a href="https://renesassynergy.com/mcuglossary">renesassynergy.com/mcuglossary</a>
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Application projects	<a href="https://renesassynergy.com/applicationprojects">renesassynergy.com/applicationprojects</a>
Self-service support resources:	
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Knowledgebase	<a href="https://renesassynergy.com/knowledgebase">renesassynergy.com/knowledgebase</a>
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## Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Aug 2, 2018	-	Initial release
1.01	Aug 8, 2018	-	Second release
1.02	Aug 30, 2018	-	Third release
1.03	Sep 14, 2018	-	Forth release

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