



software



Since 2001 Clarinox Technologies has worked towards the facilitation of more efficient embedded development. The company has developed a range of technologies by following international standards such as those published by the Bluetooth SIG and IEEE802.11 specifications.

Clarinox has developed middleware, software tools and protocol stacks. Using these proven resources, engineers can efficiently design, implement and debug complex embedded wireless products or systems.

Clarinox has access to cutting-edge research from our close ties with top universities, and participates in the partner programs of ARM, Express Logic, Green Hills Software, IAR, Intel, Mentor Graphics, NXP, STMicroelectronics, Texas Instruments and Wind River.



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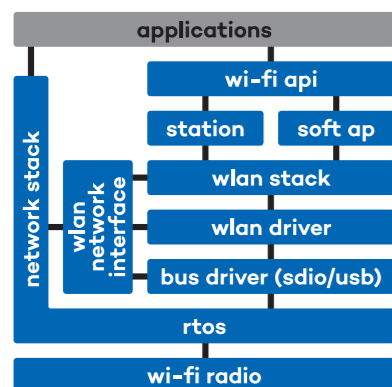
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ClarinoxWiFi Protocol Stack is the only stack with WPA Enterprise support on RTOS/MCU

- Supports AP, STA and P2P modes
- Supports multiple simultaneous roles
- Clean architecture isolates application from lower layers; can be used with any OS and TCP/IP stack
- Supports a wide range of embedded platforms
- Enables single and multi-threaded applications
- Support for blocking and non-blocking API calls
- Built-in protocol analysis tool
- Suitable for a range of IoT applications such as infotainment, navigation, video streaming, data transfer and health & medical devices



Features

Security Architecture, SoftAP, SoftMAC, Supplicant Support

Revision

2007, 2009, 2012

Core Protocol

IEEE802.11a/b/g/n/i/r

Protocols

CCMP, EAPOL (802.1x), TKIP, TKIP/CCMP

Security/Standard*

WPA/WPA2 Personal WPS EAPOL (802.11x) TKIP
WPA/WPA2 Enterprise CCMP MAC

Roles

AP, STA, P2P client and GO

Supported Chipset Vendors

Texas Instruments WiLink8,
Marvell 88w8xxx

Roadmap

Revision IEEE802.11 h/s,
Wi-Fi Aware, Wi-Fi Mesh

*Please see www.clarinox.com for the full list of supported protocols.



ClarinoxBlue™ Smart-Ready implements a number of application specific profiles and services for the Bluetooth Low Energy Specification. Custom profiles and services are also supported.

Featuring auto-generated GATT and Bluetooth SIG profiles, the ClarinoxBlue protocol stack significantly reduces development times and human errors.

ClarinoxBlue™ supports a range of OS/RTOS, CPUs and wireless vendor chips. A change of target is easily facilitated without a lengthy porting process.

Support for dual-mode Bluetooth/BLE or single-mode BLE is available.

Profiles/Services

AIOP	AIOS	ANP	ANS	BAS	BCS
BMS	BLP	BLS	CGMP	CGMS	CPP
CPS	CSCP	CSCS	CTS	DIS	ESP
ESS	FMP	GAP	GLP	GLS	HIDS
HOGP	HPS	HRP	HRS	HTP	HTS
IAS	IPS	IPSP	LLS	LNP	LNS
NDCS	OTP	OTS	PASP	PASS	PLXP
PLXS	PXP	RSCP	RSCS	RTUS	ScPP
SCPS	TIP	TDS	TPS	UDS	WSP
WSS	Custom				

Protocols

ATT GATT SM

Versions

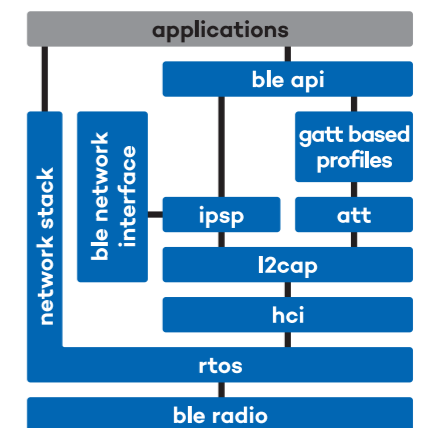
Qualified at core specification v4.0, v4.1

Qualification

Declaration ID D023635, D023636

Roadmap

2017: V5.0; MESH networking



Clarinox provides an abundance of profiles so that you have more freedom to develop leading edge designs.

ClarinoxBlue Bluetooth Protocol Stack empowers embedded developers with a simple and flexible solution, enabling them to spend more time on their application rather than the inner workings of Bluetooth technology.

- Support for single-mode or dual-mode Bluetooth/BLE
- Multiple simultaneous profiles
- Multiple simultaneous roles
- Separates applications from profiles
- Supports blocking and nonblocking API calls
- Enables single and multi-threaded applications
- Integrates command/response based APIs
- Award-winning Clarinox Debugger and Protocol Analyzer for fast development
- Jannal configuration tool for embedded software engineers developing Bluetooth and Wi-Fi
- Suitable for applications in consumer, home automation, industrial, automotive, health and medical

Profiles

A2DP	AVRCP	BIP	BPP	CTN	DI
DUN	FTP	GAP	AVDP	HCRP	HDP
HFP	HID	HSP	MAP	MPS	OPP
PAN	PBAP	SDAP	SPP		

Protocols

AVCTP	AVDTP	BNEP	HCI	L2CAP
MCAP	OBEX	RFCOMM	SDP	

Versions

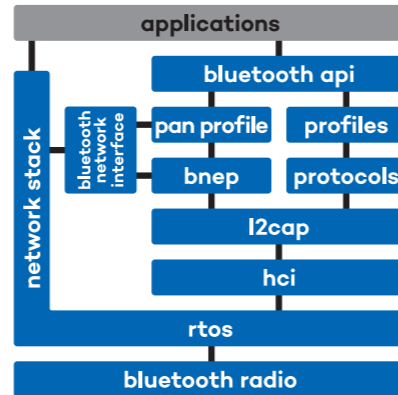
2.0, 2.1+EDR, 3.0, 4.0, 4.1 & 4.2

Qualification

Declaration ID B012420, B014172, B014173, D023635, D023636

Roadmap

2017: V5.0



Clarinox Softframe secure wireless platform - run Bluetooth, BLE and Wi-Fi together on MCU/RTOS.

The aim of Softframe is simple; to enable the electronic engineering tasks associated with the development of wireless devices to be performed efficiently, and the outcome to be more robust.

Softframe features

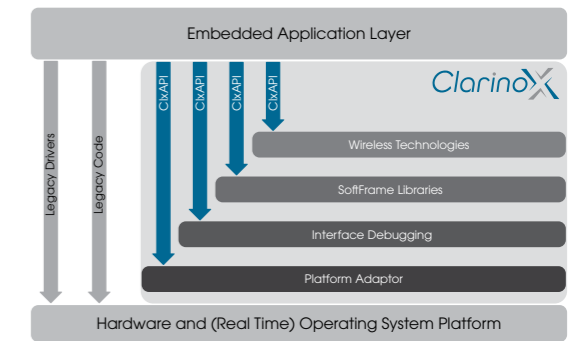
- Solid foundation with embedded security for embedded designs
- Wired/wireless protocol stacks
 - Bluetooth, BLE & Wi-Fi
- RTOS/OS abstraction functionality
 - Change target platform midproject without difficulty
 - Debug on desktop prior to custom hardware completion
 - Prevent total rewrite when targets become redundant
 - Develop for multiple platforms with a single team
- Memory leak detection
 - Prevents memory fragmentation
 - Assists to find memory leaks
- Improved system visibility and faster debugging
- Applications and wireless stacks can be placed on separate processors range of configuration options

Supported hardware

Altera, Analog Devices BlackFin, ARM Cortex M0 / M3 / M4, Cypress, Intel x86 / Atom / Quark, Marvell, Mediatek, MIPS, NXP LPCxx / i.MX / Kinetis, PowerPC, Qualcomm, Realtek, Renesas, Risc-V, SPARC-LEON, STMicro STM32F4x, TI DSP / MSP / OMAP / Tiva, Xilinx

OS/RTOS

Android, Apple iOS, eCos, embedRTOS, embOS, FreeRTOS, INTEGRITY, Linux, MQX, Nucleus, QNX, RTX, TI-RTOS, ThreadX, uC/OS-III®, uITRON, VxWorks, Windows 7 / 8 / 10, WP7 / WP8



debugger

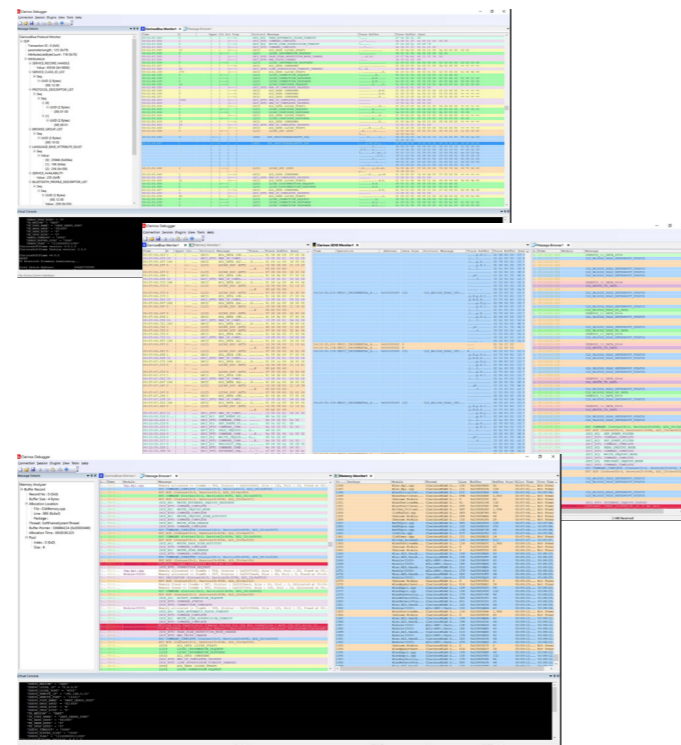
Clarinox debug tools provide in-built protocol analyser support for faster debugging of complex wireless devices. In addition, it offers threading, memory usage and memory leak analysis. Together these tools support the tuning of applications and aid in the communication of issues. The user is able to add custom plug-ins as required, with a console interface via a single physical medium.

The Clarinox Debugger provides API messaging between two processors when the stacks and applications reside on separate processors. The output of these debugger features may be provided over Ethernet, UART or custom connections.

Users communicate possible issues by storing and exchanging debugger log files with Clarinox.

These debug tools are simple to use and easy to follow, reducing overall debug times. Plug-ins can pass specific messages to the debug tools sent by the debug target. By defining plug-ins via the DLL-based plug-in interface, flexibility is provided for developers to add their own debugging functionality.

Every engineer has access to a full protocol analyzer allowing great savings.



The software component of designs is consuming larger and larger portions of product development budgets. Adding wireless into the requirement mix just adds further complexity.

Over time, Clarinox observed this industry trend and devised software systems with the goal of decreasing the burden of complexity that is placed upon the embedded software engineer. The result is a suite of protocol stacks, middleware, software debug tools and Jannal -configuration manager. This software was constructed with the aim of providing guidance, support and easier debugging for embedded software engineers.

Jannal is an IDE; but not as you currently know them. Jannal is an Intelligent Design Environment that complements, and works alongside, existing Integrated Development Environments.

Jannal is a portal to the Clarinox Bluetooth and Wi-Fi protocol stack software and the Clarinox software debug tools.

Clarinox has aligned with major RTOS, CPU and wireless component suppliers in the embedded industry to enable a range of choices between target platforms in terms

of both hardware and software. Clarinox handles the complexity for projects using multiple target platforms; or when there's a need to change platform during the product life cycle.

Jannal provides convenience by facilitating a standard approach to embedded wireless developments.

Efficient testing and evaluation of various hardware/software alternatives reduces the technical risk and helps to ensure the chosen solution is optimal.

Clarinox's Jannal Intelligent Design Environment frees the software developer from the intricate details of hardware and RTOS interface, so that attention can be focused on the application layer. In addition, this tool provides supporting intelligence such as reports and design warnings to improve productivity.

This new generation of Intelligent Design Environment allows engineers to develop embedded wireless devices without the need to learn the entire underlying system architecture. This enables them to quickly utilise the Clarinox expertise. The outcome is to allow the development team to experiment with various solutions for the end application.